Performance projections for ballistic carbon nanotube field-effect transistors

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The performance limits of carbon nanotube field-effect transistors (CNTFETs) are examined theoretically by extending a one-dimensional treatment used for silicon metal–oxide–semiconductor field-effect transistors (MOSFETs). Compared to ballistic MOSFETs, ballistic CNTFETs show similar $I-V$ characteristics but the channel conductance is quantized. For low-voltage, digital applications, the CNTFET with a planar gate geometry provides an on-current that is comparable to that expected for a ballistic MOSFET. Significantly better performance, however, could be achieved with high gate capacitance structures. Because the computed performance limits greatly exceed the performance of recently reported CNTFETs, there is considerable opportunity for progress in device performance. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1474604]

Recent demonstrations of carbon nanotube field-effect transistors and circuits suggest that these devices could play an important role in future electronic systems.[1–4] Previous theoretical studies of nanotube devices have mostly focused on two terminal devices, such as *PN* junctions and Schottky diodes,[5–7] but from an application point of view, the transistor is the most interesting. To date, experimentally fabricated carbon nanotube field-effect transistors (CNTFETs) have employed channel lengths of several hundred or thousand nanometers and often display a large contact resistance between metal and nanotube. In addition, it is not yet clear how these devices operate. One possibility is that the gate field modulated the width of a barrier at the source contact, analogous to the Schottky barrier metal–oxide–semiconductor field-effect transistor (MOSFET).[8] In this letter, we theoretically evaluated the performance limit for CNTFETs by extending the one-dimensional (1D) theory of ballistic MOSFETs to ideal, ballistic CNTFETs. We show that the characteristics of ballistic CNTFETs are affected by the 1D nature and nonparabolic band structure of the nanotube. The results indicate that reported CNTFETs operate well below the upper limit and suggest that improved technology (e.g., low resistance contacts, better gate electrostatics, and shorter channel lengths) will produce substantial performance improvements. Finally, we compare ideal, ballistic CNTFETs to ideal, ballistic MOSFETs in order to examine the role for CNTFETs in low-voltage, high-density, digital applications.

The modeled device, a coaxially gated, *N*-type CNTFET with nanotube diameter $d=1$ nm, insulator thickness $t_{\text{ins}}=1$ nm, and dielectric constant $\kappa=4$, is schematically shown in Figs. 1(a) and 1(b). The intrinsic nanotube channel is separated from the source/drain metal contact by the heavily *N*-doped nanotube source/drain extension to minimize the Miller capacitance between gate and source/drain electrode. The source/drain region could also be realized by using weakly coupled metal-nanotube contacts with an appropriate metal work function.[9] We assume that the metal-nanotube contact resistance, $R_C=0$, and carrier transport through nanotube is ballistic (no scattering). Calculations base on these assumptions should establish the upper limit of CNTFET performance.

We calculate the ballistic limit $I-V$ characteristics of a CNTFET by a procedure analogous to Natori's treatment of the ballistic silicon MOSFET.[10–13] The procedure begins by calculating the equilibrium charge density, Q_L, versus gate voltage, V_G, by solving the Poisson equation self-consistently with the carrier population in the carbon nanotube.[14,15] Above the threshold voltage, V_T, the charge in the nanotube increase approximately linearly with the gate voltage. In a long-channel transistor, the charge density at the

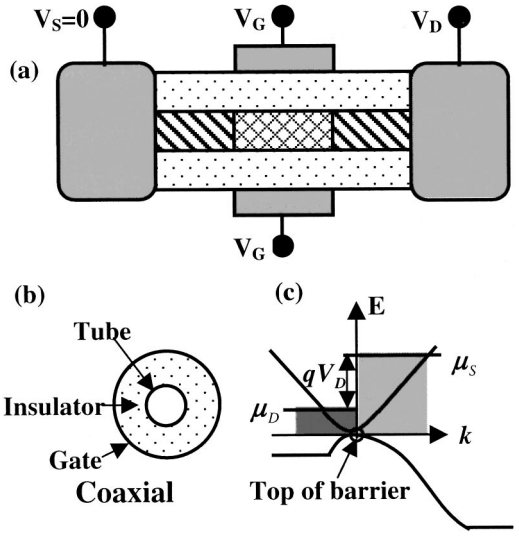

FIG. 1. Schematic diagrams of the modeled, coaxially gated CNTFET. (a) Cross section along the nanotube channel direction. The hatched line regions are the heavily *N*-doped nanotube source and drain, and the thin cross-hatched line region is the intrinsic nanotube channel. (b) Cross section perpendicular to the nanotube channel direction, which shows the gate configuration. (c) The subband profile vs the position along the channel direction. At the top of barrier, the $+k$ states and the $-k$ states are populated according to the source Fermi level μ_s and the drain Fermi level μ_D, respectively.

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beginning of the channel, Q_L, is equal to its value at equilibrium and is independent of the drain voltage. In an electrostatically well-designed, short-channel transistor, Q_L is approximately independent of drain voltage, except that the value of V_T may be shifted by two-dimensional electrostatics.[15] We may, therefore, assume that an appropriately shifted, equilibrium Q_L vs V_G relation holds at the top of the source-channel barrier. The magnitude of the resulting V_T is selected to achieve the specified I_{off}. This approach captures the essential physics of the device, but a two- or three-dimensional solution of Poisson's equation will be necessary to evaluate the magnitude of the V_T shift and the output conductance, and to address the scaling limit for CNTFETs.[16]

At the top of the barrier, the $+k$ states are populated by injection from the source and the $-k$ states by injection from the drain, as shown in Fig. 1(c). Therefore, the electron density for the ith conduction band is

$$n_i = \int_{E_0+\Delta_i}^{+\infty} \frac{D_i(E)}{2}[f(E-\mu_S)+f(E-\mu_S+qV_D)]dE, \tag{1}$$

where μ_s is the source Fermi level and, $f(E)$ is the Fermi function, and the density of states is[17]

$$D_i(E) = \frac{8}{3\pi bt}\frac{|E-E_0|}{\sqrt{(E-E_0)^2-\Delta_i^2}}\Theta(|E-E_0|-\Delta_i), \tag{2}$$

where $b \approx 1.44$ Å and $t \approx 2.5$ eV are the C–C bonding distance and energy, respectively, and $\Theta(x)$ equals 1 for positive x and 0 otherwise. The parameter, E_0, is the middle gap energy, and Δ_i is the bottom of the ith conduction band relative to E_0.[17] Summation of electron densities over all conduction bands gives the total electron density. If we set the source Fermi level to zero, then the only unknown in the above expressions is E_0. Its value is adjusted iteratively to maintain the previously computed, shifted equilibrium charge density, $Q_L(V_G)$. Finally, having determined E_0, the currents in the positive and negative half k states are evaluated by integration over energy, and their difference gives the drain current. The details of this procedure and its validation by detailed simulations are discussed by Natori[10,11] and Lundstrom.[16]

Figure 2 shows $I-V$ characteristics of the ballistic, coaxially gated CNTFET assuming a power supply voltage of 0.4 V, which is appropriate for high density, digital applications in the future.[18] The left axis of Fig. 2(a) shows the computed $\log(I_D)$ vs V_G. As noted earlier, the value of the threshold voltage was selected (by adjusting the gate electrode work function) to produce 10^{-2} μA of off-current. (The off-current specified for 2016 node of ITRS, $I_{\text{off}} = 10$ μA/μm,[18] times the nanotube diameter, $d = 1$ nm.) The on-current is 11.2 μA, well-below the 25 μA obtained for metallic nanotubes[19] because of the limited amount of charge that can be induced with a low power supply voltage and the modest dielectric constant assumed. Comparisons with conventional, planar MOSFETs are difficult because of the difference in device geometries, but we note that the on-off current ratio ($I_{\text{on}}/I_{\text{off}} \approx 1120$) outperforms that of a 10 nm ballistic MOSFET with the same insulator and power supply ($I_{\text{on}}/I_{\text{off}} \approx 110$).

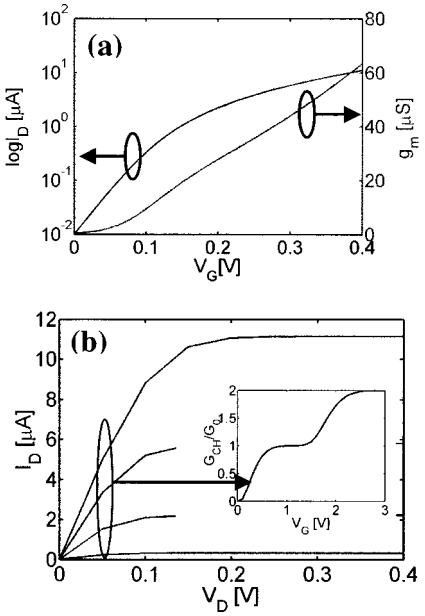

FIG. 2. $I-V$ characteristics of the coaxially gated CNTFET. (a) Computed $\log(I_D)$ vs V_G (on the left axis) and transconductance vs V_G (on the right axis) at $V_D = 0.4$ V. (b) The computed I_D vs V_D characteristic with gate bias as a parameter. ($V_G = 0.1-0.4$ V, 0.1 V/step.) The inset shows the quantized channel conductance vs gate voltage at $T = 300$ K. The normalization conductance $G_0 = 4e^2/h$, where e is the electron charge and h the Planck constant.

The right axis of Fig. 2(a) shows that the transconductance of the coaxially gated CNTFET at $V_G = 0.4$ V is 63 μS, about two orders of magnitude larger than the value reported in a recent study[2] (~ 0.342 μS) due to two reasons. First, our use of coaxial geometry with thin insulator offers better gate controlled electrostatics and about an order of magnitude larger C_G than the planar geometry with thick gate insulator used in Ref. 2. Second, the average carrier velocity at the top of the barrier ($\sim 2.7\times 10^7$ cm/s) of the ideal, ballistic CNTFET is larger than the value ($\sim 6\times 10^5$ cm/s) in the experimental CNTFET, which has a channel length of about 1 μm and is likely to be affected by scattering. The larger g_m of the ballistic, coaxial CNTFET suggests that better electrostatic design and downscaling the device, would allow it to operate closer to the ballistic limit and substantially improve its performance.

The drain current saturation displayed in the output characteristics [Fig. 2(b)] occurs (as for a ballistic MOSFET) when the drain bias is large, so that negative k-states at the top of the barrier are not occupied. The inset in Fig. 2(b) shows, however, that the low-bias channel conductance, G_{CH}, versus gate voltage behaves differently than that of a MOSFET. For a MOSFET in the degenerate limit, $G_{\text{CH}} = M(2e^2/h)$, where M is the number of occupied transverse modes.[20] Because the width of a MOSFET is typically large, the number of transverse modes, and therefore G_{CH}, increases continuously with gate voltage. For the CNTFET, however, the channel conductance versus gate voltage is quantized in units of $G_0 = 4e^2/h$, because only two modes per subband can propagate. (This effect has been discussed by Yamada.[21]) The transition between conductance steps is broadened at room temperature such that for low voltage operation, the channel conductance is approximately proportional to gate voltage.

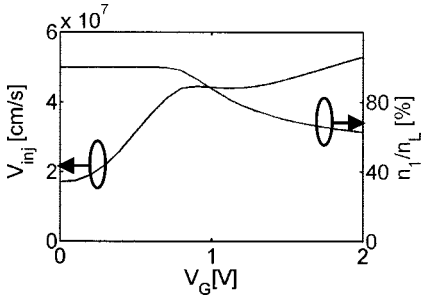

FIG. 3. The injection carrier velocity (on the left axis) and the percentage of charge in the first subband n_1/n_L (on the right axis) vs the gate voltage at $V_D=1$ V for the coaxially gated CNTFET.

Because the charge at the beginning of the channel is determined by metal–insulator–semiconductor electrostatics, it is useful to express the on-current as the product of charge times the injection velocity $[v_{\mathrm{inj}} \equiv I_{\mathrm{on}}/Q_L(0)]$, which is simply the average carrier velocity at the top of the barrier. Figure 3 plots the injection velocity (on the left axis) and the percentage of charge in the first subband (on the right axis) versus gate voltage at $V_D=1.0$ V. Under low gate voltages ($V_G<0.8$ V), the relatively small amount of charge at the top of the barrier occupies only the first subband. As the gate voltage increases from $V_G=0$ V, the Fermi level, E_F, moves to a steeper part of the band, and the injection velocity increases rapidly until E_F hits the bottom of the second subband. The band structure of a carbon nanotube allows higher injection velocities than that for silicon MOSFETs, but only at high gate voltages for which the Fermi level is well above the bottom of the first subband.

Finally, we compare the idealized, ballistic CNTFET to an idealized, ballistic single-gate silicon MOSFET with the same gate insulator thickness and dielectric constant. This comparison is most readily done for the planar nanotube array. We assume the nanotube diameter $d=1$ nm, insulator thickness $t_{\mathrm{ins}}=1$ nm, dielectric constant $\kappa=4$, and spacing between neighboring nanotube $S=2d$.[2] (Reducing the spacing to $S=d$ does not double the device performance because each nanotube image to a narrower width on the gate plane.[14]) The gate work functions of the planar CNTFET and MOSFET are adjusted to produce $I_{\mathrm{off}}=10\ \mu\mathrm{A}/\mu\mathrm{m}$.[10] The resulting ballistic on-current of the planar CNTFET at $V_{DD}=0.4$ V, 790 μA/μm, is less than that for the silicon MOSFET, 1100 μA/μm. The difference occurs for two reasons. First, when the gate oxide is thin, an array of cylindrical nanotubes (with charge almost uniformly distributed around nanotubes because most of the charge occupies the first subband) is not as effective as the planar silicon MOS capacitor in gating charge into the nanotube array.[14] Second, although the nanotube band structure allow a upper limit of $v_{\mathrm{inj}} \approx 8\times10^7$ cm/s (carrier velocity in graphene), at $V_G=0.4$ V the limited amount of charge only occupies the bottom of the first subband and results in $v_{\mathrm{inj}} \approx 1.8\times10^7$ cm/s.

The performance of the CNTFET, with respect to silicon MOSFETs, may be improved with better gate electrostatics. For example, insulators applicable to CNTFETs (e.g., Al_2O_3, dielectric constant of 9.4) can have higher dielectric constant than SiO_2 and imbedding the nanotube in the gate insulator may increase C_G somewhat.[4] Such changes improve the gate capacitance and result in comparable ballistic on-current to silicon MOSFETs. Even more effective electrostatic gating may allow the CNTFET to outperform the MOSFET. For example, the coaxially gated CNTFET delivers an on-current (11.2 μA) that much higher than the on-current per nanotube for the planar array (1.6 μA). The use of a higher dielectric constant would also benefit the CNTFET, and if high gate voltages can be used, the ballistic currents should be substantially greater than that of a corresponding MOSFET because both the injection charge density and velocity increase.

In summary, the ballistic limit performance of CNTFETs was evaluated. The $I-V$ characteristics are similar to those of a conventional MOSFET, except for the occurrence of a quantized channel conductance. The on-current and transconductance of the computed ballistic CNTFET are well above the values currently being obtained experimentally (due to our assumption of ideal metal-nanotube contacts, ballistic channel transport, and better gate controlled electrostatics), suggesting possibility to improve the performance substantially by better device design. For low voltage operation, the ballistic CNTFET with a planar gate geometry shows no advantage over the ballistic silicon MOSFET in terms of on-current, significantly better performance, however, is achieved with a coaxially gated geometry.

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