Nano Devices (EEL 5091)

Project Report
(Single Electron Devices and Circuits)

Hybrid CMOS - Single Electron Transistor (SET) Integrated Circuits

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Single electron transistors (SET’s) are of increasing interest not only from the fundamental point of view but also for their potential room-temperature application to very high density memory and logic circuits with conventional silicon VLSI processing techniques. They have unique characteristics and functionality like unrivalled integration and low power, which are complementary to the sub-20 nm CMOS. It is shown that combination of CMOS and SET in hybrid ICs appears to be attractive in terms of new functionality and performance, together with better integrability for ULSI, especially because of their complementary characteristics. It is envisioned that efforts in terms of compatible fabrication processes, packaging, modeling, electrical characterization, co-design and co-simulation will be needed in the near future to achieve substantial advances in both memory and logic circuit applications based on CMOS-SET hybrid circuits.

As in the case of the conventional CMOS circuit design, the modeling of devices and the simulation of the circuit would be a key step to design the SET circuits. Coulomb island in single-electron circuits can be treated independently when the interconnections between single electron transistors are large enough. In these regions the SPICE model is made use of. For the application of full conventional simulation techniques to single-electron circuits, parameter-based compact modeling is essential for the characteristics of isolated SET’s. But the drawbacks would be the sacrifice of the accuracy and the limited applicable regime of characteristics. It will be studied how SPICE macromodeling of single-electron transistors can be used for efficient circuit simulation.

Research Groups/ Experts in this area:

**Macromodeling of Single-Electron Transistors for Efficient Circuit Simulation**
Yun Seop Yu, Student Member, IEEE, Sung Woo Hwang, Member, IEEE, and Doyeol (David) Ahn, Senior Member, IEEE

**Analytical Modeling of Single Electron Transistor for Hybrid CMOS-SET Analog IC Design**
Santanu Mahapatra, Student Member, IEEE, Vaibhav Vaish, Christoph Wasshuber, Kaustav Banerjee, Senior Member, IEEE, and Adrian Mihai Ionescu, Member, IEEE

**Few Electron Devices: Towards Hybrid CMOS-SET Integrated Circuits**
Adrian M. Ionescu, Michel J. Declercq Santanu Mahapatra Swiss Federal Institute of Technology Lausanne Kaustav Banerjee ,Center for Integrated Systems Stanford University Jacques Gautier CEA-DRT – LETI/DTS –CEA/GRE

**SET-based nano-circuit simulation and design method using HSPICE**
Fengming Zhang, Rui Tang, Yong-Bin Kim*
Department of Electrical and Computer Engineering, Northeastern University, Boston

**SET/CMOS Universal Literal Gate – based Analog-to-Digital Converter**
Myung-Jo Chun, and Yoon-Ha Jeong, Department of Electronic and Electrical Engineering Pohang University of Science and Technology, Pohang, Kyungbuk, Republic of Korea

**A New Design Technique of Hybrid SET/MOS Static Memory Cells**
Bong-Hoon Lee and Yoon-Ha Jeong, Department of Electronic and Electrical Engineering Pohang University of Science and Technology, Pohang, Kyungbuk, Republic of Korea