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CARBON NANOTUBE FIELD-EFFECT TRANSISTORS

JING GUO*, SIYURANGA O. KOSWATTA, NEOPHYTOS NEOPHYTOU, AND MARK LUNDSTROM

Electrical and Computer Engineering, Purdue University, 465 Northwestern Avenue, West Lafayette, IN 47907, USA
lundstro@purdue.edu

**Electrical and Computer Engineering, University of Florida, Gainesville, FL 32611, USA*

This paper discusses the device physics of carbon nanotube field-effect transistors (CNTFETs). After reviewing the status of device technology, we use results of our numerical simulations to discuss the physics of CNTFETs emphasizing the similarities and differences with traditional FETs. The discussion shows that our understanding of CNTFET device physics has matured to the point where experiments can be explained and device designs optimized. The paper concludes with some thoughts on challenges and opportunities for CNTFET electronics.

Keywords: Carbon nanotubes, CNTFET, nanodevice simulation.

1. Introduction

Since the first reports of single-walled carbon nanotubes (CNTs) in 1993,[1,2] they have been the subject of intense interest for basic and applied research. Carbon nanotubes are sheets of graphene (a semi-metal) rolled into a tube.[3] Depending on the way the sheet is rolled up (its chirality) the CNT may be metallic or semiconducting.[3,4] Interest in carbon nanotubes is driven by their exceptional electronic, optical, thermal, and mechanical properties.[3,4] Semiconducting nanotubes are direct bandgap semiconductors with $E_G \approx 0.8/D$ eV, where D is the nanotube diameter in nanometers. Typical diameters are 1-2nm, and the resulting bandgaps are suitable for room temperature electronics. Low-field transport is near-ballistic with mobilities as high as ~20,000 cm^2/V-s (corresponding mean-free-paths greater than 1 μm).[5, 6] The direct bandgap means that they are optically active, so optoelectronic devices are possible.[7,8,9] The conduction and valence bands are mirror images, which is advantageous for complementary circuits. When the first carbon nanotube field-effect transistors (CNTFETs) were reported in 1998,[10,11] it was not even clear how they functioned, but subsequent progress has been rapid. CNTFET device physics is now rather well understood, and sophisticated transistor structures with high-performance operation are now being reported.[12] Our purpose in this paper is to review the current understanding of CNTFET device physics and to discuss issues and possibilities for future CNTFET technologies.

The paper is organized as follows. In Sec. II, we start with a brief summary of progress in

CNTFET technology since the first reports in 1998. Although it is not a comprehensive review, this discussion is intended to provide background for readers not familiar with CNTFET technology. As our understanding of CNTFET device physics has evolved, an ability to model and simulate them has also been developed. Section III briefly describes the device simulation approach that we use. In Sec. IV, these numerical simulations are used to discuss some key issues in device physics. Unresolved issues and possible applications of CNTFETs are discussed in Sec. V. Finally, we summarize in Sec. VI what we understand, what we still do not completely understand, and what we see as interesting potential applications for CNTFET technology.

2. Background

Manufacturing issues will ultimately play a decisive role in any future CNT electronic technology. Our focus here, however, is on the physics of CNT devices - specifically the CNTFET. It is still too early to tell what role CNTFETs will play in electronic systems of the future, but they provide us with a specific context in which to develop technology and understand transport, contacts, interfaces, etc.; which are likely to be important for CNT electronics in general. It is appropriate, however, to say a few words about where CNTFET technology stands today. Early CNTFETs were fabricated using nanotubes synthesized by a laser ablation process using nickel-cobalt catalysts.[13] The nanotubes were then suspended in a solvent and dispersed on an oxidized silicon wafer with predefined metal contact pads. The result was a random distribution of CNTs with some that bridged the contacts. Subsequently, catalytic chemical vapor deposition (CVD) methods were developed to grow CNTs on predefined catalyst islands.[14] The nanotubes thus fabricated are rooted in the catalyst islands and grow in random directions on the wafer with some terminating on another island creating bridges. CVD techniques provide more control over device fabrication and have led to rapid progress in device performance (e.g. Ref. 12).

CNTFETs are typically p-type devices that operate as so-called Schottky barrier (SB) transistors.[15] The p-type characteristics have been attributed to the alignment of source/drain metal Fermi level near the valance band of the CNTs rather than to background doping or charges.[16] The holes in the channel are electrostatically induced by applying a negative gate voltage. Transistor action occurs because the gate modulates the SB width for hole tunneling near metal-CNT contact.[16,17] While early transistors used gold (Au) as contact metals, significant performance improvements were obtained by using palladium contacts instead, which seem to eliminate the Schottky barrier for holes and produce near-ballistic operation.[18] However, other metals such as cobalt (Co) and titanium (Ti) are still being employed for high performance CNTFETs.[19,20] Metal source/drain FETs, however, still operate differently from the traditional metal-oxide-semiconductor FET (MOSFET).[21] To make a CNTFET operate like a MOSFET, source and drain regions must be created at the two ends of the CNT by heavy doping. MOSFET operation has been reported by using field plates to induce high carrier concentrations in the source/drain extensions.[22,23,24] More recently, CNT MOSFETs with doped source/drain regions have been reported.[25,26,27] It is important to specify the type of CNTFET one is dealing with. We divide them into two broad classes; i) CNT MOSFETs,

which are analogous to the traditional silicon MOSFET, and ii) CNT MSDFETs, for metal source/drain FETs. When the Schottky barrier is large, the MSDFET operates as a classic SBFET, and when the SB is small or absent, they operate somewhere between the limits of a MOSFET and SBFET.[21]

Early CNTFETs were fabricated on oxidized silicon substrates with a back-gated geometry and a thick SiO_2 layer that resulted in poor gate control of drain current.[10,11] The use of a top-gated geometry produced immediate performance improvements.[28] Wind et al. deposited a thin dielectric layer (15-20 nm) on top of CNTs, and lithographically defined metal electrodes for gating and contacts. A transconductance ($g_m = dI_{ds}/dV_{gs}|_{Vds}$) of 3.25 μS and subthreshold swing ($S = ln(10)\ [dV_{gs}/d(ln(I_{ds}))]$) of 130 mV/decade were obtained, which was a significant improvement in device performance.[28] Later, the incorporation of high-κ dielectrics in a top-gated structure produced even better device characteristics.[29] Javey et al. employed a high-κ ZrO_2 (κ ~ 25) gate dielectric with a thickness of ~ 8 nm and obtained $g_m \approx 12$ μS and $S \approx 70$ mV/decade.[29] Although not always with top-gated geometry, other groups have also reported the use of high-κ dielectrics such as HfO_2 (κ ~ 11), TiO_2 (κ ~ 40-90), $SrTiO_3$ (κ ~ 175), and even-electrolyte gating mechanisms for attaining improved performances.[17,20,30,31,32] In the case of electrolyte gating, Siddon et al. have reported $S \approx 62$ mV/decade which is very close to the theoretical limit of 60 mV/decade.[32] All of these devices appear to operate as CNT MSDFETs, some with essentially no barrier and others with rather large (half bandgap) barriers.

The possibility of ballistic operation of CNTFETs has been a topic of great interest. Since there are no dangling bonds in CNTs, surface scattering can be expected to be negligible. Back-scattering by acoustic phonons is suppressed by symmetry arguments related to the CNT bandstructure[33,34] and by the reduction in phase space for one-dimensional conductors. The result is that mean-free-paths of several hundred nanometers are commonly observed.[33,35] Under high bias, however, optical or zone boundary phonons may be emitted, and the mfps decrease substantially. Yao et al. showed that for long metallic CNTs, the current saturates at about 25 μA per nanotube.[33] They showed that the high-field current is limited by the emission of optical or zone boundary phonons with $\hbar\omega_0 \approx 200$ meV and that the high-field mfp is ~ 10nm. Yao's results suggest that for short nanotubes, comparable in length to the mfp, the current should exceed 25 μA per nanotube. This expectation was confirmed by Park et al [36] and Javey et al,[35] who both showed that the current increases above 25 μA when the length of the nanotube is less than several mfps long. By analyzing their data, both Park and Javey extracted an mfp of ~10 – 15 nm, which was consistent with the value extracted by Yao for long nanotubes. The mfps deduced from these experiments are considerably shorter than the values of 50nm or so, which are estimated from the expected electron-phonon coupling strength.[33,36] Although these results are for metallic nanotubes, similar effects are expected for semiconducting nanotubes and CNTFETs. For a tube much shorter than the mfp, carrier transport in the tube is quasi-ballistic, and the tube resistance is nearly length-independent. In contrast, a tube much longer than the mfp behaves like a classical resistor, in the sense that the resistance is proportional to the tube length.

Several recent improvements to CNTFET design collectively incorporate various techniques that have been developed during the past few years. For instance, Javey et al. reported a self-aligned top gate structure that uses the catalytic CVD method for CNT growth, a thin

HfO_2 top gate dielectric ~ 50 nm in length and self-aligned palladium source/drain contacts.[12] A transconductance of 30 μS, subthreshold swing of 110 mV/decade, and a saturation current of ~25 μA at a power supply of V_{DD}~1V were obtained.[12] Novel CNTFET device structures that enable high current operation [37] and high integration densities [38] have also been reported. These devices are all of the metal source/drain (MSDFET) variety, but it is recognized that the use of a metal source will limit the drain current (unless the SB is sufficiently negative).[21] Very recently, CNT MOSFETs with doped source/drain regions have been reported.[24-27] Substitutional doping is not practical because of the strong carbon-carbon bond, so charge transfer approaches analogous to modulation doping in III-V heterostructures [26,27,39] are used.

Although progress in CNTFETs has been rapid, there are still many issues to address. The potential for digital logic [40,41] was demonstrated early on. Techniques that modify the behavior of the nanotube from p-type to n-type have been implemented, which allowed their use in complementary CMOS logic. Following this, Derycke et al. demonstrated an inverter structure based on nanotubes.[40] Other nanotube based elementary digital logic gates with high gain and high I_{on}/I_{off} ratios, such as a NOR gate, a ring oscillator and an SRAM cell, have also been implemented.[41]

With respect to RF performance, measurements [42-44] and modeling [45-47] have both been initiated to assess performance potential. Experimental work includes that of Frank and Appenzeller,[42,43] who developed a technique to circumvent the low-current-drive problem of CNTFETs to place a lower bound on the frequency response. Li et al.[44] measured the microwave reflection coefficient from a load comprised of a nanotube and a matching circuit and demonstrated transistor operation at 2.6 GHz. In terms of modeling, Burke [45,46] has suggested an RF circuit model for a metallic nanotube, and emphasized the importance of both quantum capacitance and kinetic inductance. More recently,[47] Burke used a standard formula, along with estimated and measured values for the parameters, to predict the unity-current-gain frequency (f_T) of CNTFETs, and suggested the f_T would be given by 80 GHz divided by the tube length in microns [$f_T = 80\ GHz / L(in\ \mu m)$]. However, as we discuss near the end of this paper, much more needs to be done to definitively characterize the RF behavior of CNTFETs.

A pressing issue that limits logic and RF device performance has to do with contacts. Good contacts to the valence band are achieved by using palladium. The barrier height is approximately zero for relatively large diameter nanotubes (D ~ 1.7 nm). Achieving small barrier contacts to the small diameter nanotubes that will be necessary for room temperature operation (D ~ 1nm) is a key challenge, as is also achieving good, low barrier, contacts to the conduction band. CNT MOSFETs, however, are expected to deliver significantly better performance than MSDFETs, and recent progress on stable, heavy doping of CNTs is encouraging.[25,26,27] For many (perhaps most) applications, high currents are needed, so innovative structures that place several CNTs in parallel will be required. If these problems can be addressed, manufacturing challenges will move to the forefront. The key challenges are control of chirality and development of low temperature growth processes to allow CNTFETs to be placed at low cost on CMOS substrates. For the remainder of this paper, our focus will be on the physics of CNTFETs. Before we examine device physics, we first describe the simulation techniques that we use to explore and understand device physics.

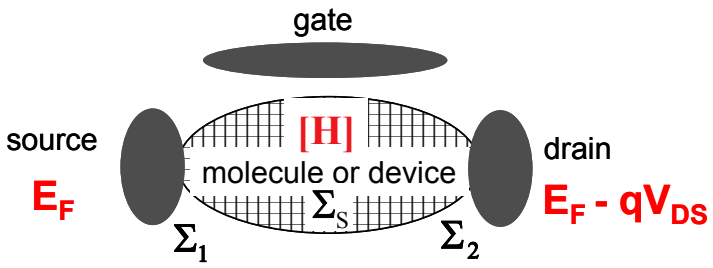

Fig. 1. A generic transistor comprised of a device channel connected to source and drain contacts. The source-drain current is modulated by a third electrode, the gate. The quantities involved in the NEGF formalism are also shown.

3. CNTFET Device Simulation by the NEGF Approach

A number of groups have reported modeling and simulation studies of CNTFETs (some examples are Refs. [17], and [47-53]). Our intent in this section is not to review that work. Instead, we briefly describe the techniques we currently use to simulate CNTFETs, because the results of our simulations will be used in Sec. 4 to illustrate key features of CNTFET device physics.

Detailed treatment of carbon nanotube electronics requires an atomistic description of the nanotube along with a quantum-mechanical treatment of electron transport. For ballistic transport, we self-consistently solve the Poisson and Schrödinger equations using the non-equilibrium Green's function (NEGF) formalism.[54] To test the validity of the simulation, we compare simulated results to a recently-reported CNTFET.[12] The comparison shows that the self-consistent quantum simulation captures the essential physics of the CNTFET. Electron-phonon scattering does occur under modest bias [35] and can be simulated by semiclassical, so-called Monte Carlo techniques,[55] but scattering has a rather small role on the dc performance of CNTFETs with a channel length less than 100nm.[56]

To correctly treat transport in carbon nanotube transistors, we need to include quantum mechanical tunneling through the Schottky barriers at the metal-nanotube contacts, and quantum tunneling and reflection at the barriers within the nanotube channel. The non-equilibrium Green's function (NEGF) formalism provides a sound approach to describe ballistic and dissipative quantum transport.[54,57] Figure 1 describes the essence of the technique and the key parameters of the formalism. The approach begins by identifying a suitable basis set and Hamiltonian matrix for the isolated channel. The self-consistent potential, which is a part of the Hamiltonian matrix, is included in the diagonal components of **H**, which is an N x N matrix where N is the total number of orbitals in the simulation domain (i.e. the number per carbon atom times the number of carbon atoms in the channel). The second step is to compute the so-called self-energy matrices, $\mathbf{\Sigma}_1$, $\mathbf{\Sigma}_2$, and $\mathbf{\Sigma}_S$, which describe how the channel couples to the source and drain contacts, and to the scattering process. For simplicity, only ballistic transport is treated in this paper, so $\mathbf{\Sigma}_S \equiv 0$. The third step is to compute the retarded Green's function,

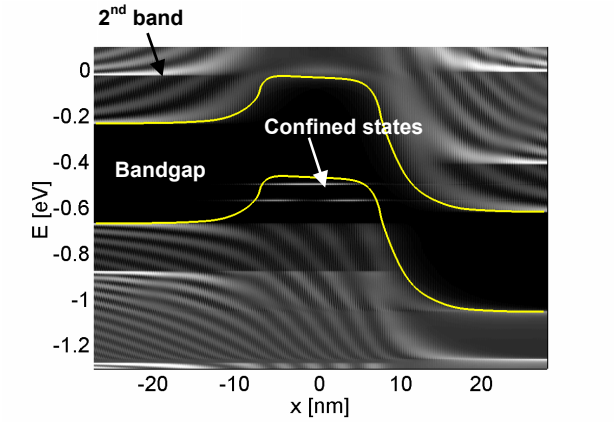

Fig. 2. The computed local density of states for a CNTFET under high gate and drain bias. Light areas indicate a high density of states.

$$\mathbf{G}(E) = [(E + i0^{+})\mathbf{I} - \mathbf{H} - \mathbf{\Sigma}_1 - \mathbf{\Sigma}_2]^{-1}. \tag{1}$$

The fourth step is to determine the physical quantities of interest from the N x N Green's function matrix. For example, the position-resolved electron density in the device is

$$n(z) = \int dE \left\{ LDOS_1(x,E) f_1(E) + LDOS_2(x,E) f_2(E) \right\}, \tag{2}$$

where $f_{1,2}$ the equilibrium Fermi functions of the two contacts, and $LDOS_{1,2}$ is the local density of states fillable by contact 1 or contact 2, which are obtained from the retarded Green's function [eqn. (1)]. For a self-consistent solution, the NEGF transport equation is solved iteratively with the Poisson equation until self-consistency is achieved. After that the source-drain current is computed from

$$I = \left(\frac{4e}{h}\right) \int T(E)[f_1(E) - f_2(E)]dE \,, \tag{3}$$

where $T(E) = \mathrm{Trace}(\mathbf{\Gamma}_1 \mathbf{G} \mathbf{\Gamma}_2 \mathbf{G}^{+})$ is the transmission between the source and the drain, $\mathbf{\Gamma}_{1,2} = i\left(\mathbf{\Sigma}_{1,2} - \mathbf{\Sigma}_{1,2}^{+}\right)$, and the extra factor of two in (3) comes from the valley degeneracy in the carbon nanotube energy band structure.

The NEGF approach as described above can be implemented by using an atomistic basis set that consists of the p_Z orbitals of all the carbon atoms in the channel. This approach produces a matrix whose size is the total number of carbon atoms in the nanotube, which makes it computationally intensive. Figure 2, which plots the computed local-density-of-states (*LDOS*) at on-state, shows that the simulation captures all important quantum effects. A mode-space

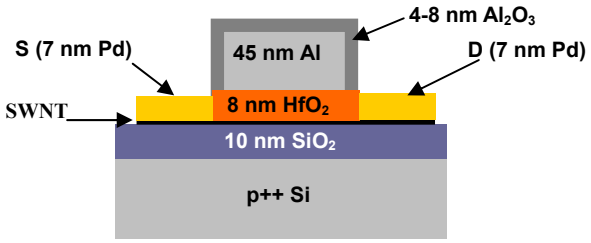

Fig. 3. A recently reported CNTFET with Pd source and drain contacts and a 50nm-long channel.[23] The HfO_2 top-gate insulator is 8nm thick with a dielectric constant $\kappa \approx 16$. The diameter of the intrinsic carbon nanotube channel is $d_{CNT} \approx 1.7$ nm. The Pd source and drain contact thickness is 7nm.

approach that significantly reduces the size of the Hamiltonian matrix when the potential around the tube is nearly invariant has also been developed.[56] It is similar to an approach that has been used for nanoscale MOSFETs.[58] It is exact for coaxially gated CNTFETs, and it also applies to CNTFETs with planar gates when the potential variation around the tube is small compared to the subband energy spacing. In brief, the idea is to exploit the fact that in a carbon nanotube, periodic boundary conditions must be applied around the circumference of the nanotube, so transport can be described in terms of these circumferential modes. Mathematically, we perform a basis transformation on the (n, 0) zigzag nanotube to decouple the problem into n one-dimensional mode-space lattices. Since only a few modes are typically involved in transport, the size of the problem is dramatically reduced, and routine device simulation and optimization becomes possible. See Refs. 56 and 59 for a detailed discussion of this approach.

In addition to the NEGF treatment of carrier transport, the device simulation requires that it be coupled to a solution of Poisson's equation for self-consistent electrostatics. Details of the electrostatic solution and coupling to the transport equation are discussed in Ref. 59. Most

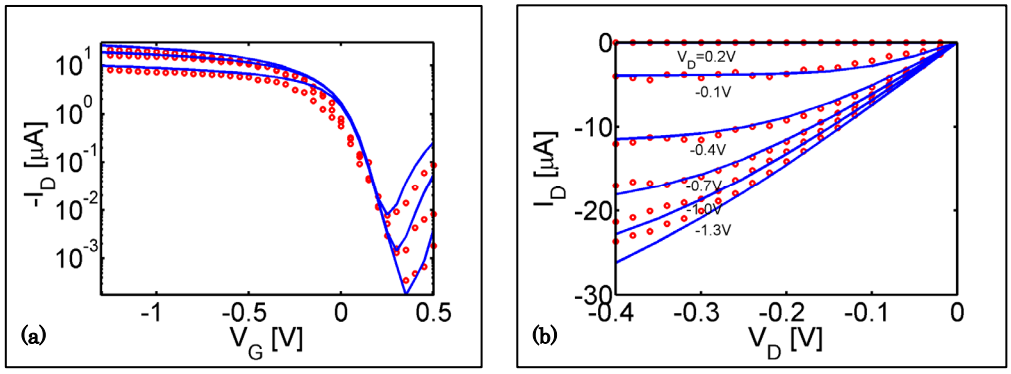

Fig. 4. Experimental (circles) and simulated (solid lines) (a) I_D vs. V_G at V_D=-0.1, -0.2, and -0.3V and (b) I_D vs. V_D characteristics. The CNT work function $\Phi_{CNT} = 4.7$ eV, the Al top-gate work function $\Phi_{Al} = 4.1$ eV, and the p^+ doped bottom-gate work function $\Phi_{pSi} = 5.1$ eV. No interface and oxide charges are included. The simulated I_D-V_G curves are translated by *+0.75*V along the *x*-axis to match the experimental curves.

CNTFETs contain a Schottky barrier at the source and drain. An atomistic treatment of the contact is not practical for device simulation, so a phenomenological treatment has been developed.[56,59] The overall technique has been used to simulate a recently-reported CNTFET as shown in Fig. 3.[12] A self-aligned gate process was used to achieve a channel length of 50nm with a D = 1.7nm CNT. A high-κ top gate insulator was used to maximize the gate modulation, and low-barrier contacts ($\Phi_{bp} \approx 0$) to the valence band were used at the source and drain to optimize the metal-nanotube contacts. This transistor demonstrates excellent on-state performance with I_D ~20 μA and a near-ideal channel conductance of $0.5 \times 4e^2/h$ achieved at a gate overdrive $|V_G - V_T|$~1V. Figure 4 plots the experimental (circles) and theoretical (lines) current-voltage characteristics. The parameters used in the quantum simulation were obtained from separate electrical measurement and characterization. The results show that the simulation is adequate to model the experimentally measured current-voltage characteristics. In the next section, we will use numerical simulations to discuss the physics of CNTFETs.

4. Device Physics of CNTFETs

Much has been learned about the device physics of CNTFETs since their first demonstration only a few years ago; our objective in this section is to summarize our current understanding of CNTFET device physics. Figure 5 illustrates two different ways to make a transistor. In the traditional MOSFET (Fig. 5a), the source and drain regions are heavily doped and an electrostatic potential barrier that prevents current flow occurs in the channel. A positive gate voltage pushes the barrier down and allows current to flow. In the so-called Schottky barrier FET (Fig. 5b), the source and drain contacts are metallic. Below threshold, the potential barrier in the channel looks much like that in a MOSFET, but above threshold, a Schottky barrier exists between the source and the channel. Transistor action occurs because the gate voltage modulates the tunneling current by modulating the width of the barrier. Because there is a tunneling barrier at the source, one should expect the on-current of a Schottky barrier FET

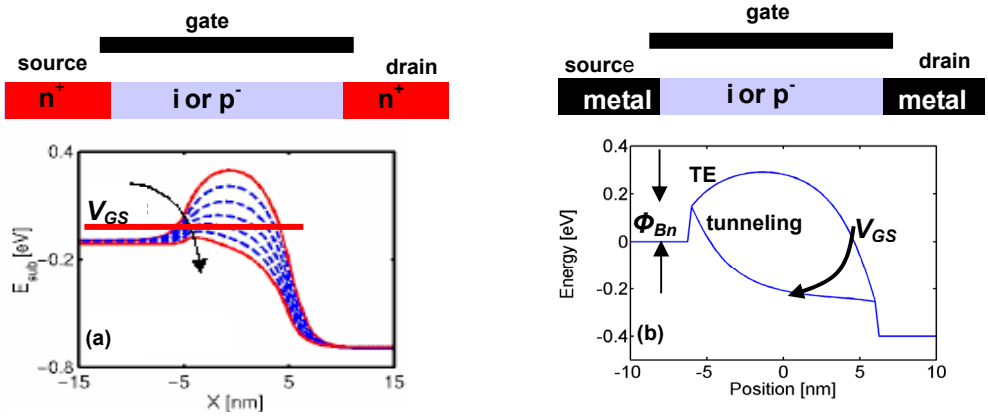

Fig. 5. Illustration of two kinds of transistors. (a) the traditional MOSFET, and (b) a metal source/drain (or Schottky barrier) FET.

to be lower than that of a traditional MOSFET. Metal contacts with essentially no barrier to the valence band can be produced (the Pd-CNT contacts of Javey et al.[18]), but it is not enough to reduce the barrier height to zero, because even then a significant fraction of the current is carried by electrons below the Fermi level which must tunnel into the semiconductor.[21] In fact, for a typical MOSFET, the Fermi level in the n^+ source and at the beginning of the channel is well above the conduction band, which is effectively a negative Schottky barrier.[21] Because metal source/drain FETs may operate with or without an actual Schottky barrier, we prefer the more general term, metal source-drain FET (MSDFET) for such devices.

Figure 6a shows the (simulated) I-V characteristics of the type that are typically observed for MSDFETs with mid-gap Schottky barriers. For $V_{GS} > V_{DS}/2$, the device is a Schottky barrier FET that operates by electron tunneling, but for $V_{GS} < V_{DS}/2$, it is a Schottky barrier FET that operates by hole tunneling. The energy band diagram at $V_{GS} = V_{DS}/2$ (Fig. 6b) shows that the device is symmetrical at this bias: electron tunneling with the left contact as the electron source, (with $V_{GS} = +V_{DS}/2$) and hole tunneling with the right contact as the hole source (with $V_{GS} = -V_{DS}/2$.). Strong tunneling occurs in these devices because of the small effective mass and the thin barriers.

The minimum current of a SB CNTFET can be shown to be [60]

$$I_D = \frac{8ek_BT}{h}\langle T\rangle e^{-(E_G - qV_{DS})/2k_BT}, \tag{4}$$

where $\langle T\rangle$ is the average current transmission coefficient. Ambipolar FETs can be used for digital logic, but the leakage current increases the standby power.[61] Acceptable leakage currents require a bandgap of at least ~0.8eV (a nanotube diameter of less than 1 nm). Another possibility for suppressing ambipolar conduction is to use a metal with a small barrier to the conduction band for the n-FET and another metal with a small barrier to the valence band for the p-FET. This approach is not very successful because the small effective masses and thin barriers produce strong tunneling.[62] Thick gate insulators lead to thick barriers that do suppress ambipolar conduction when the Schottky barrier is off mid-gap, but thick gate insulators lead to poor FET performance.[62] Clever ideas that produce a thick oxide at the drain end and a thin one at the source have been explored,[63] but it is not clear how manufacturable

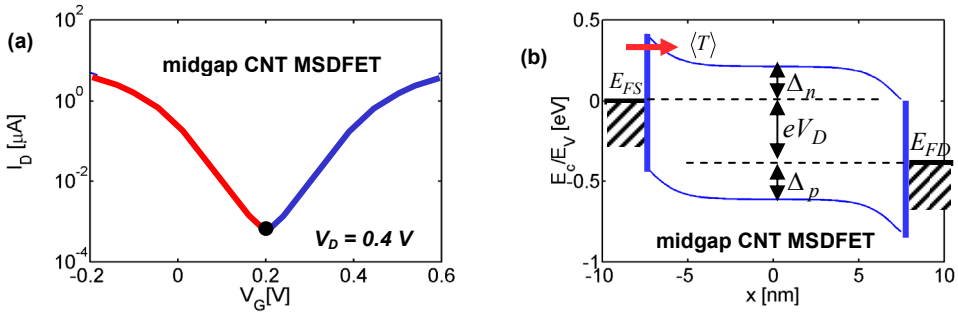

Fig. 6. Operation of a mid-gap Schottky barrier transistor. (a) the log (I_D) vs. V_{GS} characteristic, and (b) the energy band diagram at $V_{GS} = V_{DS}/2$.

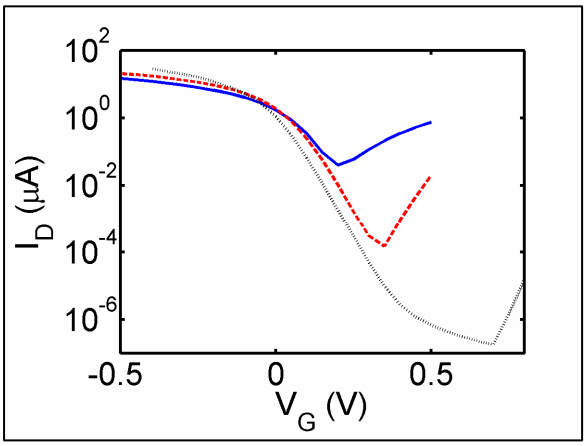

Fig. 7. The log(I_D) vs. V_{GS} plots comparing of three type of CNTFETs sat V_{DS} = 0.4V. Solid line: the CNT MSDFET device of Javey et al.[12] Dashed line: simulation of a similar CNT MSDFET but with a small diameter nanotube (1.0 nm instead of 1.7 nm) and a thinner HfO_2 gate insulator (4nm instead of 8 nm). Dotted line: Simulation of a CNT MOSFET with the same nanotube diameter and gate insulator as in the dashed line.

such approaches would be.

The achievement of carbon nanotube MOSFETs would provide improved on-current and suppress ambipolar conduction. Figure 7 illustrates what may be possible; it compares a recently reported p-type MSDFET in which the barrier to the valence band is approximately zero [12] to two simulations. The first simulation is for a MSDFET similar to [12] but with a smaller nanotube (D = 1.0nm) and thinner gate insulator (4 nm of HfO_2). (For this simulation, we assume that a barrier height of zero to the valence band can still be achieved in the smaller diameter nanotube.) The second simulation is for a CNT MOSFET with the same diameter nanotube and the same gate insulator. The CNT MOSFET is seen to offer higher on-current and lower off-current. Ambipolar conduction is also observed in the CNT MOSFET, but it occurs by band to band tunneling and is orders of magnitude lower. To achieve such devices, we must learn how to efficiently dope CNTs. Substitutional doping is difficult to envision because of the strong carbon-carbon bonds, so charge transfer schemes analogous to modulation doping in III-V semiconductors is being explored. Promising results have recently been reported [25-27] and more work is underway.

The interest in CNTFETs was spurred by the demonstration of exceptionally high mobilities in CNTs.[5,6] Under low bias, mean-free-paths of several hundred nanometers are observed. As discussed earlier, however, under high bias optical and zone boundary phonons can be emitted, and the mean-free-path decreases to about 10 nm. One might expect that these short of mfps would degrade the on-current of a CNTFET, but recent simulations show that this is not the case.[56] Because the optical phonon energy is so high (~200 meV), a carrier that backscatters by emitting an optical phonon does not have sufficient energy to surmount the barrier and return to the source.[56] Such carriers rattle around in the channel and diffuse out to the drain. The result is that the steady-state drain current is not affected by such scattering and the dc current is essentially at its ballistic value.

5. Discussion

During the past few years, much has been learned about the physics of CNTFETs. Sophisticated device structures with high-κ gate dielectrics and self-aligned gate electrodes are now being reported.[12] Contacts are still a challenge, especially low barrier contact to the conduction band. Techniques to achieve stable, high levels of doping will need to be developed so that high performance CNT MOSFETs can be produced. Our understanding of scattering is still incomplete; for example, the mean-free-paths computed from the expected electron-phonon coupling parameters [36,64] are longer that the value deduced from experiments.[33,35,36] Hot phonon effects, which are a possible explanation for this discrepancy, need to be explored. Scattering in doped CNTs is also not understood. Javey et al.[29] observed good transport properties after the tube is very heavily doped, but Appenzeller et al.[65] observed a significant degradation of current due to doping. The future of CNTFETs will depend on two things, finding appropriate applications and developing high volume manufacturing technologies.

Because of their excellent transport properties, RF applications of CNTFETs have been the subject of considerable recent interest.[43,44] While the dc performance of CNTFETs is now understood rather well, little is known about their RF performance. The band-structure limited velocity of ~8x 10^7 cm/s is high and leads to expectations of THz performance. We have argued that phonon scattering has a small effect on the dc current of a CNTFET, but it does lead to dispersion in the transit time and should affect the ac performance. For RF applications, the MSDFET may be suitable, because leakage currents are not as important as in high density digital circuits. We still do not understand, however, how CNT MSDFETS and CNT MOSFETs compare for high-frequency applications. Other issues, such as the role that the so-called kinetic inductance [45,46] might play in such devices, also need to be explored.

6. Summary

Carbon nanotube field-effect transistors are interesting devices with potentially important applications in electronics. In this paper, we have summarized the current status of the field in terms of fabrication technology and device physics. The rate of progress in CNTFET technology and in the understanding of their device physics has been very rapid. Although uncertainties remain, the dc performance of field-effect transistors can now be explained. During the next few years, we expect to see increased work on other devices, for example, high-speed transistors, optoelectronics devices, and bio-sensors. We are sure to learn a good deal of interesting new device physics in the process and may even discover important technological applications.

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