A Computational Exploration of Lateral Channel Engineering to Enhance MOSFET Performance

Jing Guo, Zhibin Ren and Mark Lundstrom

School of Electrical and Computer Engineering

Purdue University, West Lafayette, IN 47907 USA

Abstract: Techniques to engineer a MOSFET's channel in the lateral direction have been proposed to enhance the device performance. In this paper, we present a thorough simulation study to evaluate the feasibility of such lateral engineering techniques. Each of three types of transport equations, the ballistic Boltzmann, drift-diffusion and non-equilibrium Green's function with scattering, is solved self-consistently with 2-D Poisson equation to simulate device performance under both the ballistic and dissipative transport conditions. The results indicate that even if highly idealized device structures are assumed, only limited improvements over the conventional MOSFETs can be achieved by the channel engineering techniques. These results don't conflict with reports of large on-current improvements using the lateral channel engineering, because those comparisons with the conventional MOSFETs were done without specifying a common off-current.

Key words: lateral channel engineering, hetero-material gate MOSFETs, ballistic transport, Green's function

I. Introduction

The success of the microelectronics industry has kept the channel length of MOSFETs scaling down by a factor of 70% about every three years over the past decades. ITRS target for the on-current remains the same while that for the off-current doubles from generation to generation [1], which suggests that as the device scales down, the on-current to off-current ratio, I_{on}/I_{off}, decreases. Since larger I_{on}/I_{off} can provide faster speed and lower leakage, designing MOSFETs with enhanced I_{on}/I_{off} is of wide interest. Techniques to engineering the channel in the lateral direction to improve MOSFET performance have been proposed. The main consideration of such designs is to produce a desired profile along the channel direction as shown in Fig. 1, compared with that of the conventional MOSFETs. The modified profile can generate a larger electric field at the beginning of the channel and results in a larger carrier injection velocity, which is supposed to increase I_{on}. The potential profile can be generated by either using a gate with dual worfunctions, which is referred as the hetero-material gate MOSFET (HMGFET) [2-4], or doping the source end of the channel more heavily than the rest, which is referred as the asymmetric channel doping MOSFETs (ACDFETs) [5, 6]. Another lateral channel engineered device, the straddle gate MOSFET [7], which uses two side gate beside the inner gate with a different work function, is based on the consideration to electrically reduce the effective channel length from the off-state to the on-state. In this paper, we compare lateral-channel engineered MOSFETs and conventional MOSFETs with the same off-current and geometric specifications under both the ballistic and dissipative transport conditions. The results indicate that even if

highly idealized device parameters are assumed, only limited improvements can be achieved.

Fig. 1

II. Approach

The 2-D transport equation in the MOSFET channel region is solved by splitting it into two 1-D problems. In the direction normal to the channel, the Schrodinger equation is solved to yield subband profile and vertical electron concentration. In the lateral direction, three types of transport equations, the Boltzmann equation in the ballistic limit, drift-diffusion equation and Non-Equilibrium Green's Function (NEGF) with scattering are solved to yield electron density in the lateral direction and the source-drain current on the basis of the subband profiles. A 2D Poisson equation is solved self-consistently with each of the transport equations. Details of calculation scheme can be found in reference [8].

The ballistic limit is calculated semiclassically by solving Boltzmann equation. For each spatial point, the occupation of a state in k- space is determined by the Fermi-Dirac function with the source or drain Fermi level, depending on which contact the electrons fill such state come from. For example, at the barrier top, the positive half of k-space is filled by electrons from the source while the negative half by electrons from the drain.

In our Green's function method, we treat scattering using a simple Buttiker-probe model. Scattering centers are viewed as reservoirs similar to the source and drain. However, they differ from the source and drain reservoirs as they can only change the energy of carriers and not the total number of carriers in the system. This model has been demonstrated to capture the essential physics of scattering [8].

III. Results and Discussions

The characteristics of a conventional double-gate MOSFET at 30-nm channel length, as shown in Fig. 2(a), are calculated as the comparison baseline to evaluate the performance of HMGFETs. An ultrathin silicon body and gate oxide are assumed in order to suppress 2-D short channel effects. While 2nm Si body thickness and 1nm gate oxide thickness can hardly be achieved with current fabrication technologies and may cause problems such as the gate leakage, the purpose of exploiting such parameters is to evaluate the maximum achievable improvement of HMGFETs under highly idealized conditions. Our comparisons between HMGFETs and the conventional MOSFET are done by specifying the common geometric parameters and off-current. For HMGFETs as shown in Fig. 2(b), the off-current is kept the same with that of the conventional MOSFET by choosing an appropriate source gate workfunction, ϕ_1, and assuming the drain gate workfunction, $\phi_2 = 4.05V$. The characteristics are then simulated and compared with the corresponding ones of the conventional MOSFET.

Fig. 2

To determine the source gate length L_1, the first subband profiles of HMGFETs with different L_1 values at on-state are simulated as shown in Fig. 3. HMGFETs with short source gate length generate preferable potential profile in the consideration of maximizing the electric field near the subband barrier top. Increasing the source gate length results in the decrease of the electric field near the source, which makes the subband profile approach that of the conventional MOSFET. When the source gate length is longer than one half of the total gate length, the subband profile near the barrier top is

almost the same as that of the conventional MOSFET. HMGFETs with three different source gate lengths L_1=5nm, 10nm and 15nm are studied in the subsequent ballistic and dissipative transport calculations.

Fig. 3

Figure 4(a) shows I_{DS} -V_{GS} characteristics of HMGFETs, compared with that of the conventional MOSFET. The L_1=5nm HMGFET has a larger subthreshold swing and worse short-channel immunity. Increasing the source gate length to 10 and 15nm improves the subthreshold characteristics, which are mainly dominated by the device electrostatics. The degraded electrostatic properties associated with HMGFETs can be understood by qualitatively analyzing 2-D Poisson equation in the channel region. The slope of subband profile of HMGFETs increases from zero at the barrier top to a large value in order to increase carrier injection velocity, indicating a rapidly spatial change of electric field at the position. The rapidly varying field results in the large absolute value of the second derivative of the potential along the channel, which may invalidate the gradual channel approximation and lead to more severe 2-D short channel effects [9]. Such short channel effects cause less effective gate modulation on the barrier top of HMGFETs, especially for those HMGFETs with short source gate length. Thus the barrier top of HMGFETs cannot be pushed down so much as that of the conventional MOSFET from the off-state to the on-state. The higher subband barrier tops result in the reduction of the ballistic on-current as indicated in Table 1.

Fig. 4

In the presence of scattering, the characteristics of HMGFETs and the conventional MOSFET are first calculated using the drift-diffusion model. From the design

consideration of the lateral channel engineering, it might be expected that the largest I_{on} improvement can be achieved by L_1=5nm HMGFET because it maximize the electric field near the barrier top. However, the results indicate an opposite situation as shown in Table 1. Although the L_1=5nm HMGFET do achieve the largest carrier injection velocity V_{inj} as shown in Fig. 5(a), the injection carrier density reduction, which is shown in Fig. 5(b) is more dominant and causes the overall decrease of the on-current. Such reduction can be explained on the basis of simple gate control electrostatics, which express the injection carrier density as $Q_{inj} = C_{eff}(V_G - V_T)$, where C_{eff} is the effective gate capacitance, V_G is the gate voltage and V_T is the threshold voltage. The worse subthreshold characteristics of L_1=5nm HMGFET requires a larger V_T to yield the specified off-current, thus causing the decrease of Q_{inj} at on-state when the same C_{eff} is assumed. Increasing the source gate length can lead to larger Q_{inj}, however, at the same time, it decreases V_{inj} as shown in Fig. 5. This trade-off relation between Q_{inj} and V_{inj} makes it hard to achieve large on-current improvement. In the best case when L_1=15nm, a maximum improvement of about 10% is obtained, which is shown in Table 1.

Fig. 5

Drift-diffusion treatment misses transport mechanisms such as quantum tunneling and velocity overshoot, which can be important for small dimensions. To include physics beyond DD model, the NEGF approach with scattering was employed to recalculate the device characteristics at the on-state. A typical velocity distribution curve of HMGFET as shown in Fig. 6 displays two overshoot peaks, one at the boundary between the source and drain gate, the other near the drain end. These two peaks are related to the rapidly spatially increase of electric field at these two regions. The left velocity overshoot peak

can yield larger improvement of carrier injection velocity than the drift-diffusion model results, thus corresponding to larger on-current improvement as shown in Table 1. About 20% improvement was attained in the best case.

Fig. 6

Table 1

Since asymmetric channel doping is essentially based on the same design consideration as HMGFETs, similar observations apply to such device. The present study uses double-gate structure with extremely thin gate oxide and Si body thickness to suppress the short channel effects. If more realistic parameters are used and non-ideal conditions, such as parasitic resistance, included, the improvement achievable by using lateral channel engineering would become even smaller.

It is also worth pointing out that our results don't contradict most of the reported large improvements of on-current achieved by lateral channel engineering because these comparisons were done without specifying a common off-current. Comparing on-currents without considering the off-state or by specifying a common threshold voltage can leave the worse subthreshold performance of the lateral channel engineered MOSFETs out and lead to larger improvements. One exception reporting better subthreshold performance by exploiting hetero-material gate structure needs further study [2].

IV. Conclusions

Each of three types of transport equations is solved self-consistently with 2-D Poisson equation to compare the performance of conventional MOSFETs and HMGFETs under both the ballistic and dissipative transport conditions. The ballistic results indicate that

HMGFETs have larger subthreshold swing and threshold voltage than the conventional MOSFETs due to the short channel effects, leading to smaller on-current. After including scattering, we showed that the higher carrier injection velocity of HMGFETs due to larger electric field near the barrier top doesn't necessarily lead to larger on-current. For many cases, the lateral field gradient degrades shot channel performance, so for a specified off-current, the threshold voltage is higher, which makes the on-current smaller. When highly idealized device parameters are used, a maximum improvement of 10-20% can be achieved. Such observations can also be extended to ACDFETs, which is essentially based on the similar design consideration as HMGFETs.

References:

[1] International Technology Roadmap for Semiconductors, Semiconductor Industry Association, 1999

[2] W. Long and K. K. Chin, IEDM Tech Digest (IEEE, Washington DC, 1997), p. 549.

[3] X. Zhou and W. Long, IEEE Trans. Electron Devices, **45**, 2546 (1998)

[4] X. Zhou, IEEE Trans. Electron Devices, **47**, 113 (2000)

[5] S. Odanaka and A. Hiroki, IEEE Trans Electron Devices, **44**, 595 (1997)

[6] H. Shin and S. Lee, IEEE Trans. Electron Devices, **46**, 820 (1999)

[7] S. Tiwari, J. J. Welser and P. M. Solomon, IEDM Tech Digest (IEEE, San Francisco, 1998), p. 737.

[8] Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices (Cambridge University Press, Cambridge, UK, 1998), p. 144

[9] Z. Ren, Ph. D. Thesis, (Purdue University, West Lafayette, IN, USA, 2001), unpublished

List of Tables

Table 1: On-current evaluation of three HMGFETs using different transport models, where the units of I_{on} are $\mu A / \mu m$ and Increase indicates the percentage increase of I_{on} over the conventional MOSFET with the same transport model.

	Ballistic		DD		NEGF	
	I_{on}	Increase	I_{on}	Increase	I_{on}	Increase
Conventional	2340	--	810	--	1378	--
L_1=5nm HMG	1439	-38%	605	-25%	1248	-10%
L_1=10nm	2060	-12%	829	+2%	1615	+17%
L_1=15nm	2262	-3%	882	+10%	1643	+20%

List of Figures

Fig. 1 The conventional (solid line) and desired (dashed line) potential profile along the lateral direction of the channel. Also shown is the schematic structure of HMGFETs which can generate the desired potential profile if the source gate workfunction ϕ_1 is lager than the drain gate workfunction ϕ_2.

Fig. 2 (a) A conventional symmetric double-gate MOSFET with 30-nm intrinsic channel. An ultrathin body and oxide $t_{si} = 2nm, t_{ox} = 1nm$ and a middle gap gate workfunction $\phi_G = 4.3V$ are assumed. The top and bottom gates have equal lengths with the channel. (b) HMGFET with the same geometric dimensions. The total gate length is the sum of the source gate length L_1 and the drain gate length L_2.

Fig. 3 The potential profile along channel at the on-state for HMGFETS with different L_1. $\phi_1 = 4.4V$ and $\phi_2 = 4.05V$ are kept constant.

Fig. 4 The I_{DS} vs. V_{GS} characteristics at V_D=0.6V calculated by the ballistic transport model. Solid line: the conventional MOSFET shown in Fig. 2. Dash line: L_1=5nm HMGFET with $\phi_1 = 4.46V$. Dot line: L_1=10nm HMGFET with $\phi_1 = 4.33V$. Dash-dot line: L_1=15nm HMGFET with $\phi_1 = 4.31V$.

Fig. 5 (a) The velocity distribution and (b) the electron density along the lateral direction at on-state calculated using drift-diffusion model for MOSFETs with the same symbols as Fig. 4.

Fig. 6 The velocity distribution at on-state calculated using NEGF. for MOSFETs with the same symbols as Fig. 4.

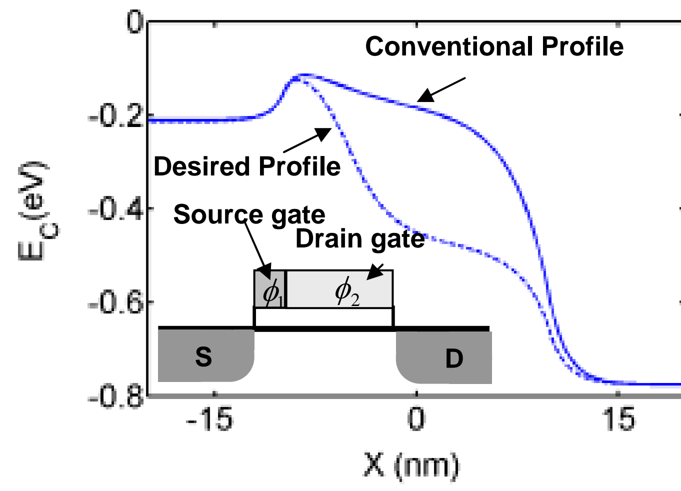
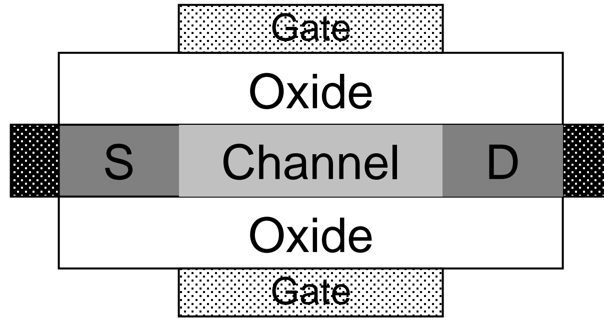
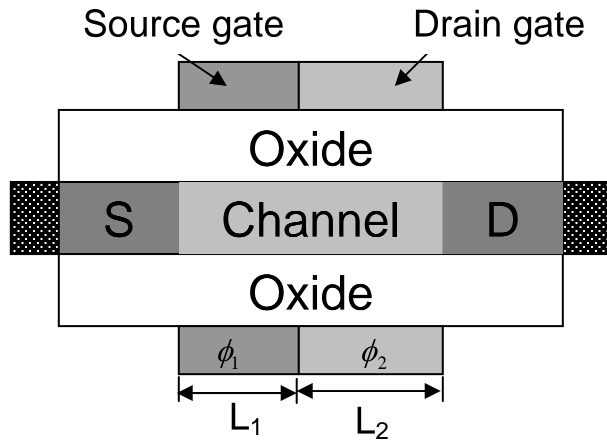


Figure 1



(a)



(b)

Figure 2

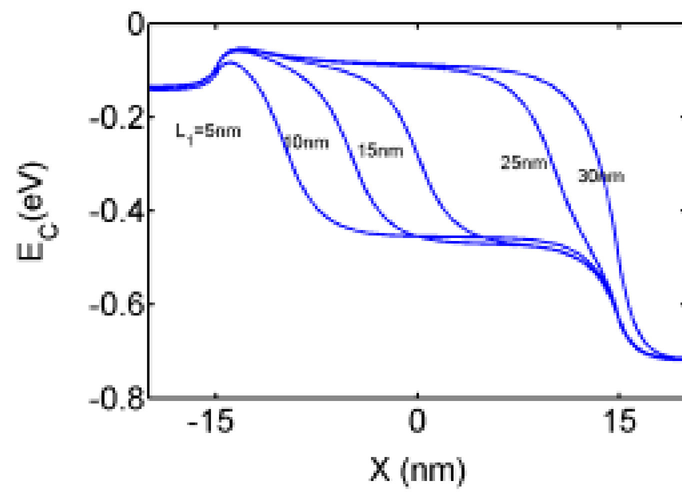


Figure 3

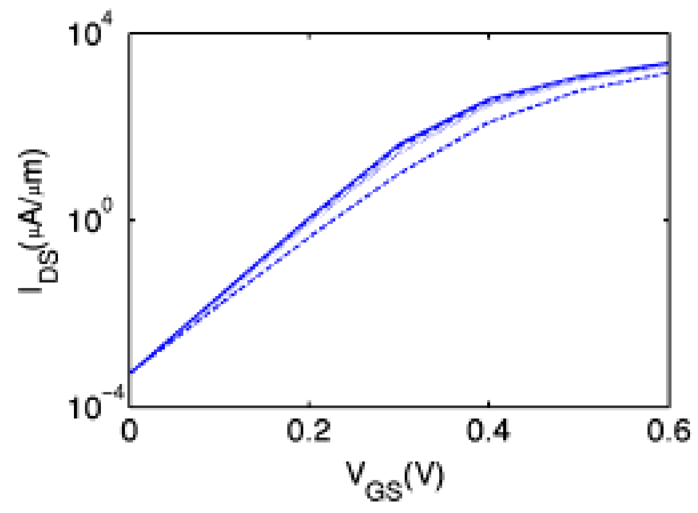


Figure 4

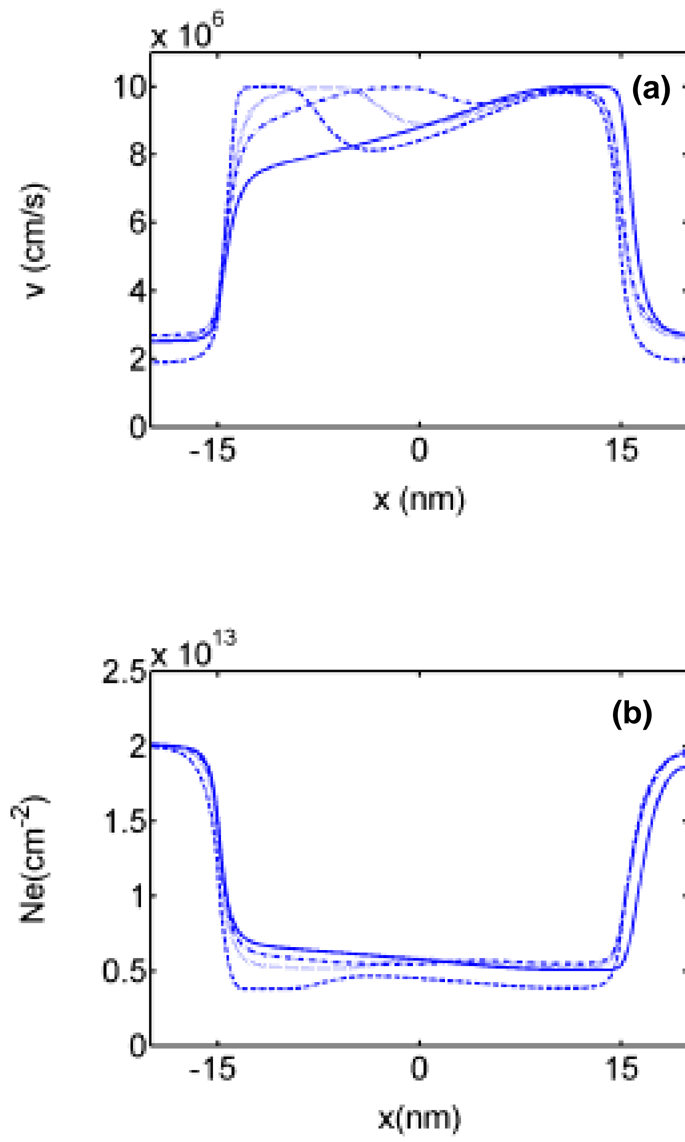


Figure 5

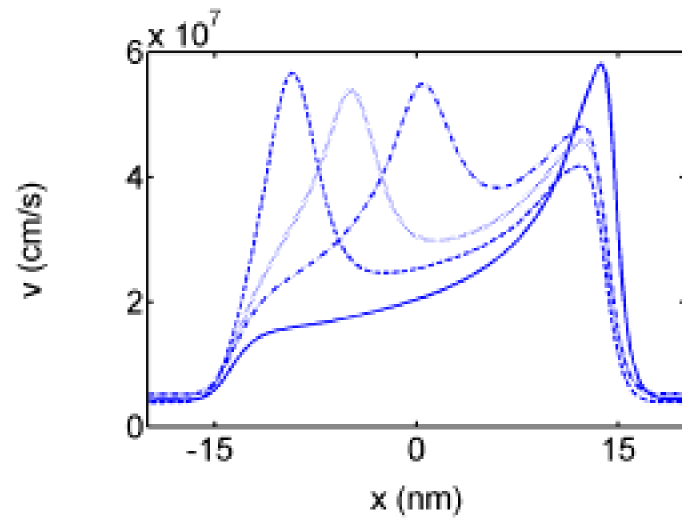


Figure 6

Affiliation of author:

Jing Guo, Zhibin Ren and Mark Lundstrom

School of Electrical and Computer Engineering

1285 Electrical Engineering Building

Purdue University, West Lafayette, IN 47907 USA

Acknowledgment

This work was supported by Semiconductor Research Corporation under the contract number 99-NJ-724.