A Computational Study of Thin-Body, Double-Gate, Schottky Barrier MOSFETs

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***Abstract*—Nanoscale Schottky barrier MOSFETs (SBFETs) are explored by solving the two-dimensional Poisson equation self-consistently with a quantum transport equation. The results show that for SBFETs with positive, effective metal-semiconductor barrier heights, the on-current is limited by tunneling through a barrier at the source. If, however, a negative metal-semiconductor barrier height could be achieved, on-current of SBFETs would approach that of a ballistic MOSFET. The reason is that the gate voltage would then modulate a thermionic barrier rather than a tunneling barrier, a process similar to ballistic MOSFETs and one that delivers more current.**

***Index Terms*—MOSFETs, nanotechnology, quantum effects, Schottky barriers, semiconductor device modeling, transistors.**

I. Introduction

THE Schottky barrier MOSFET has a similar device structure to the conventional MOSFET, but the source–drain region is made of silicide or metal rather than heavily doped semiconductor [1]–[3]. The device offers several potential advantages over a conventional MOSFET at nanometer scale. Therefore, it is being explored for scaling beyond the limit of the conventional MOSFET. From a fabrication point of view, SBFETs require no ultrahigh doping in source–drain regions, and the metal-semiconductor junctions between source–drain and channel can be abrupt [4]. These properties alleviate requirements of very steep p-n junctions and extremely high doping in the source–drain region, which are significant challenges in the fabrication of conventional, nanoscale MOSFETs [5]. From a device performance point of view, the parasitic resistance of conventional MOSFETs is expected to substantially degrade the on-current at nanoscale channel lengths [6]. By using silicide source–drain, SBFETs would essentially eliminate the parasitic resistance, and thus could deliver more on-current than the conventional MOSFET.

Bulk SBFETs suffer from large leakage currents through the body under off-state condition [7], but an ultrathin SOI body, 15-nm gate length SBFET recently demonstrated good device operation at nanoscale dimensions (an on-current of $\approx$ 200 μA/μm and an on–off ratio of $I_{\rm on}/I_{\rm off} \approx 10^4$ [3]).

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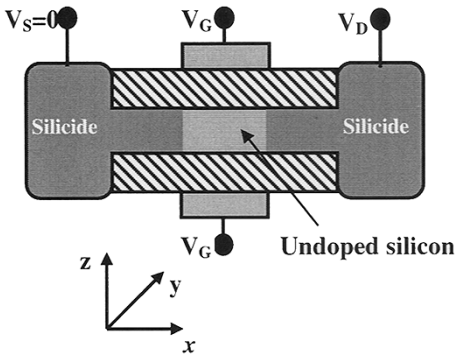

Fig. 1. Thin-body, double-gate SBFET with silicide/metal source and drain. Both the gate and channel length are 12 nm, the intrinsic silicon body thickness $t_{si} = 3$ nm, the gate-oxide thickness $t_{ox} = 1$ nm, and dielectric constant $\kappa = 4$. The coordinate system used in the calculation, which defines the longitudinal direction as x, the channel width direction as y, and the vertical direction as z, is also shown.

Theoretical studies of SBFETs have focused on assessing device operation at nanometer scale, treating the tunneling through Schottky barriers, and fitting the experimental data [2], [8]–[10]. Several questions remain. For example, how do SBFETs compare to conventional MOSFETs, what are the carrier transport mechanisms, and how should designs be optimized? In this paper, we address these questions by simulating nanoscale, double-gate, thin-body SBFETs using a quantum approach. We find that the on-current of SBFETs with positive Schottky barrier heights is limited by tunneling through the M/S barrier at the source. The effective Schottky barrier height of thin-body SOI SBFETs is higher than that of the bulk case due to quantum confinement in the direction normal to the channel. Lowering the barrier height enhances the on-current, even if a common off-current is specified. Even when the Schottky barrier height is zero, however, tunneling from the source still limits the current. The optimum barrier design requires a negative Schottky barrier height, which, if achievable, would provide the SBFET with a similar on-current and carrier transport mechanism of an ideal, ballistic MOSFET without performance degradation of the source–drain series resistance.

II. Approach

The double gate, thin body SBFET with a 12-nm gate and channel length shown in Fig. 1 was simulated by solving the two-dimensional (2-D) Poisson equation self-consistently with the Schrödinger equation using the Greens function formalism [11]. The flowchart for simulating the device characteristics at a single bias point is shown in Fig. 2. Ballistic operation was

assumed for all simulations in this paper. The 2-D transport equation in the MOSFET channel region was solved by a mode space approach that splits the problem into two one-dimensional problems [12]. In the vertical direction (z-direction in Fig. 1), the Schrödinger equation was solved for each x-position independently to generate the ith subband profile $E_i(x)$ and the corresponding wave function $\psi_i(x,z)$

$$-\frac{\hbar^2}{2m_z^*}\frac{\partial^2}{\partial z^2}\psi_i(x,z) - qV(x,z)\psi_i(x,z) = E_i(x)\psi_i(x,z) \quad (1)$$

where m_z^* is the effective mass along z-direction, q is the electron charge, $\hbar$ is the Planck's constant, and $V(x,z)$ is the electrostatic potential.

In the longitudinal direction, the nonequilibrium Green's function (NEGF) approach, which is equivalent to solve the Schrödinger equation with the open boundary condition, was used to describe the ballistic, quantum transport. The 2-D electron density is shown in (2) at the bottom of the page, where $\Im_{-1/2}$ is the Fermi integral of order $-1/2$, μ_S (μ_D) is the source–drain Fermi level, and $D_{Si}(E,x)$ ($D_{Di}(E,x)$) is the local density of states (LDOS) of the ith subband contributed by the source (drain), which is calculated based on the Green's function formalism. The 2-D electron density, $n_{2D}(x)$, is then weighted by the eigenfunction at the position x, $\psi_i(x,z)$, to get the three-dimensional electron density

$$n_{3D}(x,z) = n_{2D}(x)\cdot|\psi_i(x,z)|^2. \quad (3)$$

A 2-D Poisson equation was then solved in the silicon channel and gate oxide to update the electrostatic potential. (a nonlinear Poisson equation was solved to improve the outer-loop convergence [13]). The electrostatic potential at the contacts with gate and source (drain) electrodes were specified as boundary conditions. The iteration between the quantum transport equation and the Poisson equation was repeated until the self-consistency was achieved, then the source–drain current was calculated as shown in (4) at the bottom of the page, where I_{0i} is a constant with the dimension of current and $T_{SDi}(E)$ is the transmission from the source to drain for the ith subband at energy E, which is evaluated based on the NEGF approach. Details of the calculation scheme can be found in [13].

The simulations reported here were done within an effective mass description; we did not attempt a microscopic description of the Schottky barrier. The silicide/silicon was treated as follows. First, a virtual constant conduction band in the silicide, several tenths of eV below the first conduction band minima and the drain Fermi level, was introduced. Electrons below the virtual conduction band can rarely tunnel into the channel and have little effect on changing density and current in silicon channel, and therefore, only those electrons above the virtual band were treated. Second, the effective mass of the silicide was assumed to be the same as that of silicon, because the transport through Schottky barrier is dominated by the abrupt potential change rather than the effective mass difference. To test the sensitivity of the results to the effective mass in silicide/metal, we varied the effective mass of metal in the transport direction from $m^* = 0.1$ to 1. (The effective mass of silicide is hard to be determined because its band structure is not well known. A previous theoretical study, which assumes $m^* = 0.35$ for PtSi, a widely used silicide for p-type SBFETS, fits the experimental data well [10]). Over this range the current changed less than 5%. We verified that this procedure reproduces the conventional theory of metal/silicon Schottky barriers [4]. One should note, however, that while this simplified model produces the correct charge density and current in the intrinsic silicon channel, it should not

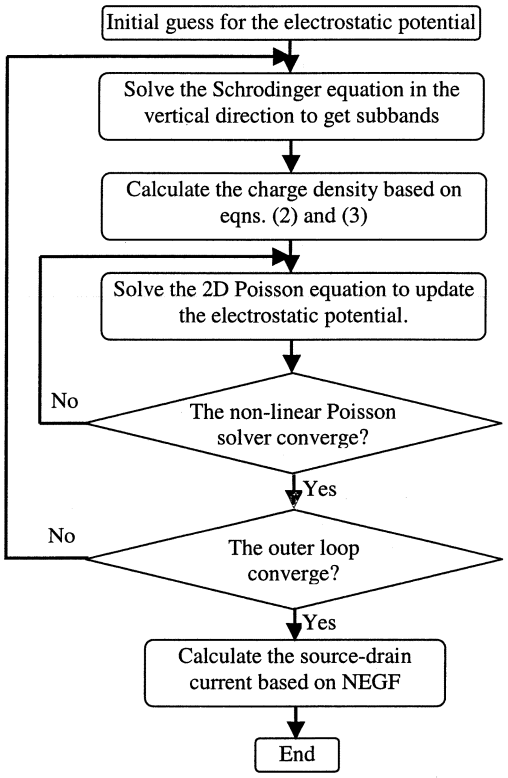

Fig. 2. Flowchart of the simulation program.

$$n_{2D}(x) = \sum_i \left\{ \int_{-\infty}^{+\infty} dE \left[\Im_{-1/2}(\mu_S - E) D_{Si}(E,x) + \Im_{-1/2}(\mu_D - E) D_{Di}(E,x) \right] \right\} \quad (2)$$

$$I_D = \sum_i I_{0i} \int_{-\infty}^{+\infty} T_{SDi}(E) \left[\Im_{-1/2}(\mu_S - E) - \Im_{-1/2}(\mu_D - E) \right] dE \quad (4)$$

be viewed as a physical, rigorous treatment of the silicide–metal junction. The Schottky barrier height, for example, was an input to the model, not an output.

III. Results

Fig. 3 displays the computed energy band diagrams for the device of Fig. 1 with a Schottky barrier height of $\phi_B = 0.1$ eV (higher barrier heights are typical in practice, but this value is sufficient to illustrate the point that Schottky barriers limit the on-current.) As discussed later, the Schottky barrier height is defined for a metal to bulk silicon junction; quantum confinement in the ultrathin body raises the effective barrier height. Under low gate voltages, the energy band diagram resembles that of a conventional MOSFET with a large energy barrier between source and drain, and the current is limited by thermionic emission over the barrier. (The gate workfunction for this device was selected to produce an off-current of 1 μA/μm.) The source–drain current is limited by the thermionic emission over the barrier in the channel and the gate modulation on source–drain current is achieved by pushing down this barrier. Under high gate bias, a conduction band spike appears at the source, and the current is limited by tunneling through the spike. Increasing the gate voltage reduces the thickness of the tunneling barrier at the source, and therefore, increases the current.

Next, we examined the performance of the device as a function of the Schottky barrier height. The first SBFET examined had a Schottky barrier height of $\phi_B = 0.1$ V, which is determined by the source–drain silicide material and the interface states. We also investigated two nonconventional SBFETs, one with zero Schottky barrier height, $\phi_B = 0$, (which we initially thought would operate like a MOSFET) and the other with a negative barrier height of $\phi_B = -0.25$ eV. A conventional, thin body, double gate MOSFET with the same geometry was also simulated to offer a comparison baseline. The gate workfunctions of all devices were adjusted to produce the same off-current, $I_{\text{off}} = 1$ μA/μm. The power supply voltage $V_{DD} = 0.4$ V, specified by ITRS for low voltage, high performance, digital applications between year 2013 and 2016, was used [14].

Fig. 4 shows that the current–voltage (I–V) characteristics of SBFETs are similar to those of conventional MOSFETs. The on-current of the $\phi_{Bn} = 0.1$ eV ballistic SBFET is the smallest, about 35% of that of the ballistic MOSFET. Lowering the barrier height to $\phi_B = 0.0$ eV improves on-current to about 50% of that of the ballistic MOSFET. This value is, in fact, comparable to that expected for a conventional MOSFET including parasitic resistance and scattering in the channel [6]. For a negative Schottky barrier height of $\phi_B = -0.25$ eV, however, the on-current of the ballistic SBFET, approaches that of the ballistic MOSFET. The results indicate that if a common off-current is specified, more on-current is delivered with lower Schottky barrier heights. As the barrier height is made progressively more negative, the on-current of the ballistic SBFET finally saturates at the same value as an ideal ballistic MOSFET. Whether or not such a negative barrier height can be obtained is problematic, but these simulations shed some light on the operating principles of a SBFET.

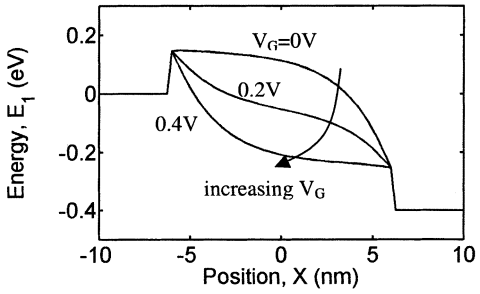

Fig. 3. The computed-energy band diagrams of the 12-nm channel-length SBFET (as shown in Fig. 1) with Schottky barrier height $\phi_B = 0.1$ eV at $V_D = 0.4$ V and $V_G = 0$, 0.2, and 0.4 *V*.

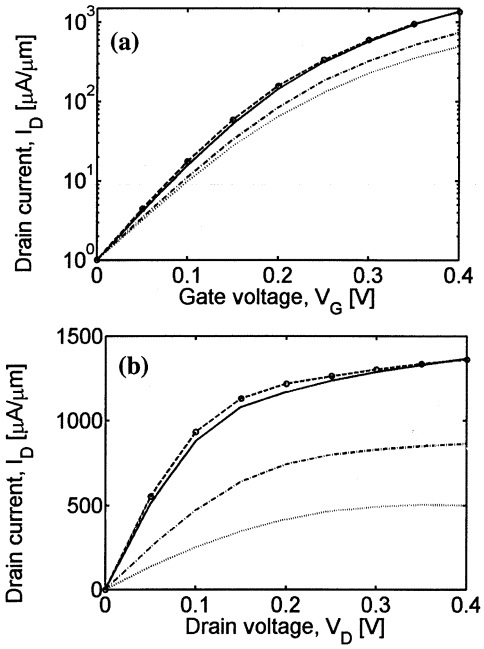

Fig. 4. I–V characteristics of three SBFETs and a MOSFET. (a) $\log(I_D)$ versus V_G characteristics at $V_D = 0.4$ V. (b) I_D versus V_D characteristics at $V_G = 0.4$ V. The solid line is the $\phi_B = -0.25$ eV SBFET, the dash-dot line is the $\phi_B = 0$ SBFET, the dotted line is the $\phi_B = 0.10$ eV SBFET, and the dashed line with circles is the conventional MOSFET.

Fig. 5(a) and (b) provide additional insights into the results of Fig. 4. As shown in Fig. 5(a) (which compares the first subband profile of these SBFETs under on-state conditions) beyond a certain gate voltage, the current of the SBFETs with positive or zero effective barrier heights is limited by the tunneling barrier at the source rather than the thermionic barrier in the channel, as it is in the negative barrier height SBFET. Somewhat surprisingly, Fig. 5(a) also shows that when $\phi_B = 0.0$ eV a tunneling barrier still exists. This occurs because we have defined the Schottky barrier height with respect to a bulk, metal/silicon junction. For this thin body device, however, quantum confinement raises the electron energy levels in the silicon, so that the effective barrier height, therefore, is

$$\phi_{eff} = \phi_B + \phi_q \tag{5}$$

where ϕ_q is the quantum confinement energy of the first subband and ϕ_B is the Schottky barrier height of a bulk M/S junction with the same material parameters and interface states.

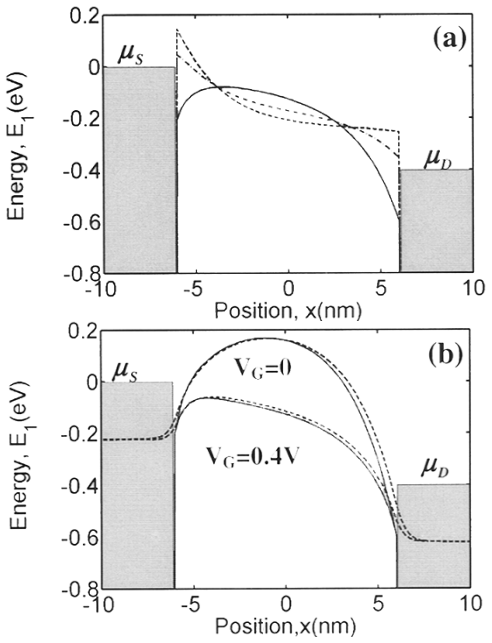

Fig. 5. The first subband profile versus position. (a) On-state of three SBFETs: the $\phi_B = 0.1$ eV SBFET (dashed line), the $\phi_B = 0$ SBFET (dash-dot line), and the $\phi_B = -0.25$ SBFET (solid line); and (b) comparison between the conventional MOSFET (dashed line) and the $\phi_B = -0.25$ eV SBFET (solid line). μ_S and μ_D are the source and drain Fermi level (for both SBFETs and the MOSFET), respectively. The shaded regions are the metal (for SBFETs) and n^+ Si (for the MOSFET) source and drain.

As the Schottky barrier height is made progressively more negative, the on-current approaches that of the corresponding ballistic MOSFET. The similarity of this device to the conventional MOSFET is shown in Fig. 5(b), which compares the energy band diagrams of the conventional MOSFET with that of the $\phi_B = -0.25$ eV SBFET. Inside the channel, especially near the top of the barrier, the energy bands of the two devices are almost the same, resulting in similar on-currents. Note that under on-current conditions, the Fermi level in the source (n^+ silicon or silicide) is above the conduction band maximum in both cases. The result is that the current is modulated by thermionic emission over a barrier rather than by tunneling through a barrier.

IV. Discussion

The fact that a negative barrier height is needed to produce a SBFET whose on-current is not limited by tunneling was not expected (it might be imagined that the zero effective barrier height is low enough to eliminate the tunneling barrier at the source, which limits the on-current). Fig. 6, which shows the first subband profile under on-state ($V_D = V_G = 0.4$ V) for the conventional MOSFET and the SBFET with zero effective barrier height, $\phi_{eff} = 0$, explains why this occurs. This figure clearly shows that the spike of the first subband profile of the SBFET, which has an energy larger than the top of the first subband of the conventional MOSFET and, thereby, limits the on-current, still exists even if the effective barrier height is reduced to zero. A substantial negative Schottky barrier height, therefore, is needed to achieve a condition in which the current is limited by thermal injection.

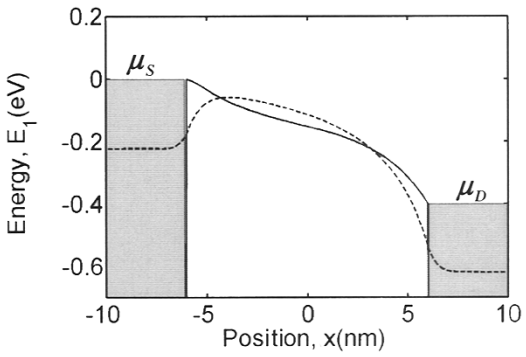

Fig. 6. First subband profile versus position under on-state conditions for two cases: the conventional MOSFET (dashed line) and the SBFET (solid line) with $\phi_B = -46$ meV (which quantum confinement increases to an effective barrier height of zero).

The need to produce a negative effective Schottky barrier height is further illustrated by viewing the source–drain barrier of the conventional MOSFET in a similar way to the SBFET. Fig. 7 shows the first subband profile, $E_1(x)$, under zero V_D, and a high gate bias. It is clear that there is an energy barrier between the source and the drain (E_1 is higher in the channel than in the source). The Schottky barrier height, however, is defined as the difference between the first subband at the source/channel interface and the source Fermi level. It is clear from Fig. 7, that this quantity is negative for the n^+-silicon/i-silicon junction, so to achieve the same energy band profile when the n^+ silicon is replaced by a metal, a hypothetical metal with a negative barrier height is necessary.

It is also important to note that with positive and negative barriers, the operating principles of the device above the threshold are different. For the MOSFET (or the negative barrier SBFET), $I_D = q n_S(0) \langle v(0) \rangle$ where $n_S(0)$ and $\langle v(0) \rangle$ are the carrier density and the average carrier velocity at the beginning of the channel (the top of the source-to-channel barrier), respectively [15]. The carrier density $n_S(0)$ is approximately independent of the drain bias in an electrostatically well designed MOSFET (or the negative barrier MOSFET). For the positive barrier SBFETs, however, there is no clear beginning of the channel where the carrier density holds approximately constant for a given gate bias. The dependence of on-current on Schottky barrier height is also different. As long as the effective Schottky barrier height is negative enough, the drain current is independent of its value. The on-current of the positive barrier SBFETs is, however, limited by the tunneling barrier and, thus, varies exponentially with the barrier height. So the devices operate differently depending on whether the effective Schottky barrier height is positive or negative.

Negative barrier heights will be difficult to achieve because barrier heights are determined by virtual gap states and defects rather than by workfunction differences [16]. One possibility to achieve negative barrier heights is to form an ultrathin oxide layer between silicon and an appropriate metal (not reactive with the oxide and with a very low workfunction). The oxide passivates the interface states and prevents Fermi level pinning [17]. It should be thick enough to passivate the surface but thin enough to transmit electrons from the contact. We also note that current work on carbon nanotube field-effect transistors with

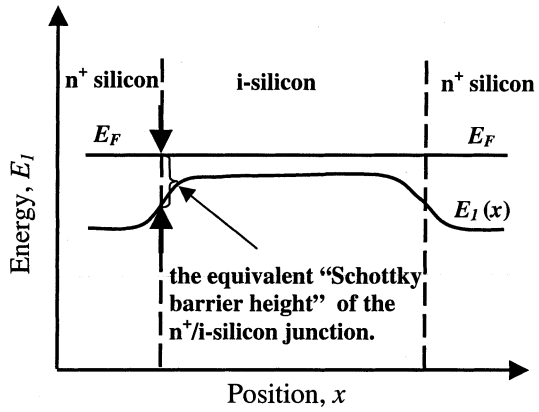

Fig. 7. Sketch of the first subband profile E_1 versus position along the channel x for a MOSFET under equilibrium conditions ($V_D = 0$, but the gate voltage is high). Note that the Fermi level is well above $E_1(x)$ in the heavily doped source. For a Schottky barrier, the "barrier height" is defined as $q\phi_B = (E_1(0^+) - E_F)$, the difference in conduction band edge in the semiconductor and the Fermi level in the metal at the junction. If we apply the same definition to the MOSFET, then the equivalent Schottky barrier height of the n^+/i-Si is clearly negative.

low workfunction metal contacts appears to be directed at a similar objective [18].

V. Conclusion

Double-gate, thin body, nanoscale SBFETs were simulated by solving the two-dimensional Poisson equation self-consistently with the Schrödinger equation. For typical SBFETs, tunneling through the metal-semiconductor barrier at the source limits the on-current. If a negative metal-semiconductor barrier height could be achieved, the ballistic SBFET could deliver the on-current of a ballistic MOSFET with essentially no parasitic resistance. Our simple treatment neglects Schottky barrier lowering, phonon- and defect-assisted tunneling, band structure effects, etc., which could increase the transmission of the barrier, but the conclusions that barriers limit performance and that optimum performance requires a negative barrier are expected to be preserved in a more detailed simulation. Nevertheless, even with a positive barrier, SBFETs could out-perform conventional MOSFETs because the series resistance, which severely degrades the performance of conventional MOSFETs at the nanoscale regime, is dramatically lower for SBFETs. Hot electrons generated at the source barrier might also increase device speed [19].

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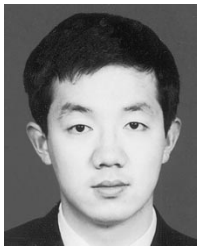

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