Assessment of Silicon MOS and Carbon Nanotube FET Performance Limits Using a General Theory of Ballistic Transistors

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ABSTRACT

A simple model for ballistic nanotransistors, which extends previous work by treating both the charge control and the quantum capacitance limits of MOSFET-like transistors, is presented. We apply this new model to MOSFET-like carbon nanotube FETs (CNTFETs) and to MOSFETs at the scaling limit. The device physics for operation at ballistic and quantum capacitance limits will be explored. Based on the analysis of recently reported CNTFETs, we compare CNTFETs to MOSFETs. The potential performance advantages over Si that might be achieved at the scaling limit are established by using the new model.

INTRODUCTION

Although carbon nanotube FETs (CNTFETs) with device performance metrics significantly above those of Si MOSFETs have recently been reported (1-4), CNTFET technology is still at an early stage: device structures are still primitive and the device physics is still relatively unexplored. In this paper, we examine recent data, identify key questions and establish the upper limit performance that might be achievable. Finally, we compare the projected performance to that of a ballistic silicon MOSFET at the scaling limit using a new, general model for ballistic nanotransistors.

Three possible types of CNTFETs are sketched in Fig. 1. The first, Fig. 1(a), is a depletion mode, p-CNTFET in which the nanotube is uniformly doped, and ohmic contacts are made at the two ends. The on-current of such a device would be limited by "source exhaustion," $I_D(on) \approx qp_L\tilde{\upsilon}_T$, where p_L is the hole density per unit length and $\tilde{\upsilon}_T$ is the uni-directional thermal velocity. The second possibility is a MOSFET-like device in which the ungated portion is heavily doped. In this case, the on-current is limited by the amount of charge than can be induced in the channel by the gate and not by the doping in the source. The third possibility is that the device operates like a Schottky barrier FET (5,6).

Schottky barrier FETs require careful alignment of the Schottky barrier and the gate electrode, which may be a manufacturing challenge, and the presence of the Schottky barrier lowers the on-current (7). Although several CNTFETs have been reported, it is not clear what type of device they are, or even if the devices being reported all operate in the same way. Because the MOSFET-like transistor [Fig. 1(b)] offers the high performance potential, we will examine its upper limit performance potential in detail.

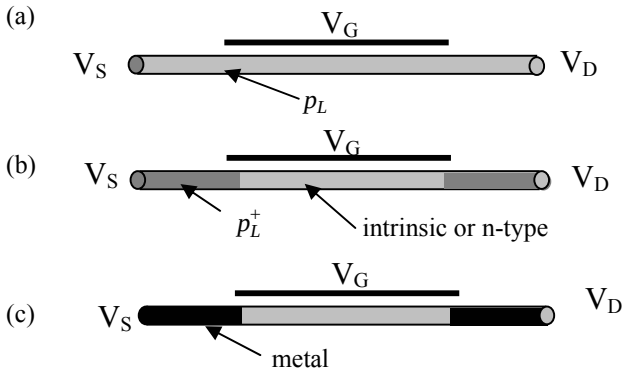

Fig. 1 Three possible types of CNTFETs: (a) p-channel depletion (b) p-channel enhancement, and (c) a Schottky barrier transistor.

Natori's theory of the ballistic MOSFET (8), which has been used to assess MOSFET performance limits for silicon MOSFETs (9), assumes that the gate voltage holds the charge at the beginning of the channel constant. This assumption works well for typical MOSFETs, but for CNTFETs with electrolyte or high-κ gating (2-4), the insulator capacitance, C_{ins}, can be significantly higher than the semiconductor capacitance, C_Q In this quantum capacitance limit, familiar MOS gate charge control concepts do not apply, and a MOSFET-like device can behave more like a bipolar transistor (11). In this paper, we extend Natori's theory to: 1) use a surface potential approach so that the semiconductor (or quantum) capacitance is included and 2) to include 2D electrostatics in an analytically simple way. Because the theory applies to both Si MOSFETs and CNTFETs, it also allows us to compare the ultimate performance of the two technologies.

THEORY

A simple model for ballistic nanotransitors is summarized in Fig. 2. The calculational procedure is:

i) Assume a V_D, and a beginning-of-the-channel nanotube potential, V_{CNT}.

ii) Relate the charge at the beginning of the channel, Q_{CNT}, to V_{CNT} and V_D by Fig. 2(c).

$$n = \int_{E_o}^{+\infty} \frac{D(E-E_o)}{2}\left[f(E-\mu_S)+f(E-\mu_D)\right]dE \,. \quad (1)$$

3) Calculate I_D from (13)

$$I_D = \frac{4ek_BT}{h}\left[\ln\left(\frac{\mu_S - E_o}{k_BT}\right) - \ln\left(\frac{\mu_D - E_o}{k_BT}\right)\right]. \quad (2)$$

4) Calculate the V_G required to produce the assumed V_{CNT} based on the the capacitance model [Fig. 2 (b)],

$$V_{CNT} = \frac{C_{ins}}{C_{ins}+C_D}V_G' + \frac{C_D}{C_{ins}+C_D}V_D' + \frac{Q_{CNT}(V_{CNT},V_D)}{C_{ins}+C_D} \,. \quad (3)$$

By repeating step 1) to 4) for a set of (V_{CNT}, V_D) points, the $I_D(V_G,V_D)$ characteristics are obtained, and interpolation is used to produce an $I_D(V_G,V_D)$ characteristic at a fixed gate voltage. The same model can be used for ballistic MOSFETs if a Si E(k) is used. This simple model was validated by solving the 2D Poisson equation self-consistently with the ballistic Boltzmann equation for both MOSFETs (14) and for coaxially-gated CNTFETs. A Matlab® script that performs this calculation is available (15).

THE QUANTUM CAPACITANCE LIMIT

To examine the MIS electrostatics of ideal CNTFETs, three different gate insulator capacitances were used: 1) C_{ins}=*0.4pF/cm* (for a ~10nm-thick, SiO_2 back gate), 2) *5pF/cm* (for a ~3nm-thick, ZrO_2 top gate (3)), and 3) *90pF/cm* (for an electrolyte gate with dielectric constant

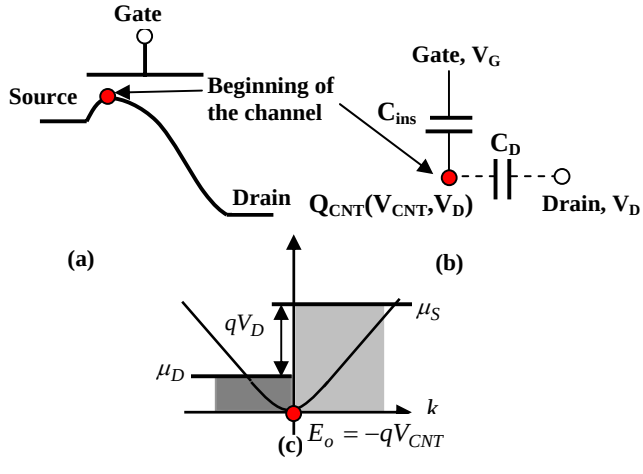

Fig. 2 (a) The subband profile *vs.* the channel position at a high drain bias and (b) The proposed model of CNTFETs. The gate voltage V_G, modulates the channel through the gate insulator capacitance C_{ins}. 2D electrostatics could be included by assuming a drain capacitance, C_D. (c) At the ballistic limit, the +k states at the beginning of the channel are filled by the source Fermi level and the –k by the drain Fermi level.

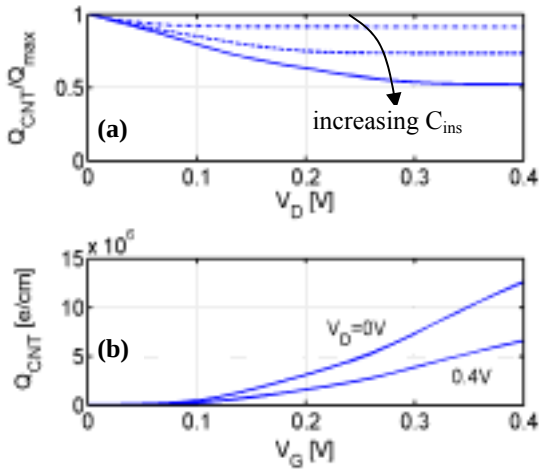

Fig. 3 (a) The normalized electron density at the beginning of the channel *vs.* the drain voltage at V_G=0.4V for three N-type, 3nm-diameter, CNTFETs with Cins=0.4pF/cm (dash-dot line), 5pF/cm (dashed line), and 90pF/cm (solid line). (b) The charge *vs.* the gate voltage curves for C_{ins}=90pF/cm. The power supply voltage specified by ITRS for the 2016 technology node [15], 0.4V, is assumed in the subsequent calculations.

$\kappa = 80$ (2, 4)). Because $C_{ins} >>> C_Q$ (estimated to be 4pF/cm if one subband occupied), the electrolyte gated CNTFET approaches the quantum capacitance limit. As shown in Fig. 3(a), when $C_{ins} << C_Q$, the charge at the beginning of the channel is nearly independent of the drain voltage, as discussed in Ref. (12). On the other hand, when $C_{ins} >> C_Q$, the charge at the beginning of the channel decreases by a factor of two as V_D increases. In the quantum capacitance limit, instead of holding the charge constant, the gate holds the nanotube potential constant at the gate potential. In this sense, the device operates more like a bipolar transistor (11). Because the nanotube potential is pinned by the gate voltage, increasing the drain bias suppresses the –k half of the distribution function and reduces the charge density by a factor of 2. At high V_D, therefore, the gate capacitance is only one-half of its equilibrium value, as shown in Fig. 3(b).

Figure 4 confirms predictions of the simple model using detailed numerical simulations that solve the ballistic Boltzmann equation self-consistently with the 2D Poisson equation. It also shows that a charge control model would greatly overestimate the drain current in the quantum capacitance limit. For typical Si MOSFETs, the charge control model is excellent, because the insulator capacitance is relatively low and the quantum capacitance, which is proportional to the semiconductor density-of-states, is relatively high. For CNTFETs, however, high- κ gate dielectrics are more readily achieved and the 1D density-of-states lowers the quantum capacitance. The result is that CNTFETs can readily operate in the quantum capacitance limit.

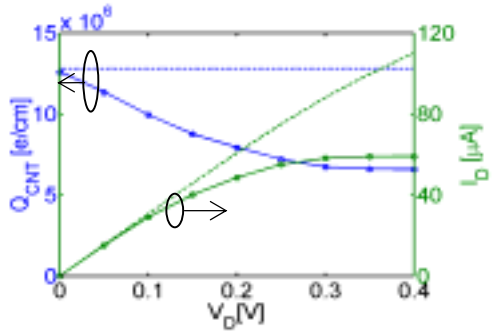

Fig. 4 The charge at the beginning of the channel (on the left axis) and the drain current (on the right axis) *vs.* the drain voltage at V_G=0.4V and C_{ins}=90pF/cm by the charge control model [8] (dashed line) and the new model (solid line). The detailed numerical simulation (circles) shows the charge control model fails at the quantum capacitance limit.

The theoretical ballistic I_D vs. V_G characteristics of three CNTFETs are shown in Fig. 5. Large currents may be possible if the channel length is much less than 10-100nm, the mean-free-path for optical phonon scattering (17). Increasing C_{ins} increases I_{on}/I_{off}, but the benefit is small if C_{ins}, is larger than C_Q.

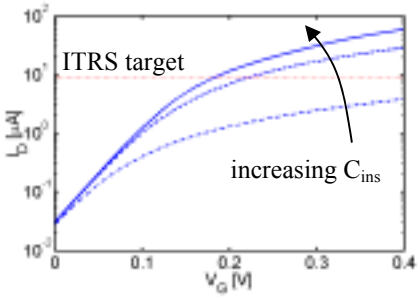

Fig. 5 The drain current *vs.* the gate voltage for C_{ins}=0.4pF/cm (the dash-dot line), 5pF/cm (the dashed line), and 90pF/cm (the solid line). The dotted line shows the ITRS target of on-current, 1500 $\mu A/\mu m$, times 2*d*, where $d = 3nm$ is the diameter of the nanotube.

Fig. 6 compares the transconductance and the channel conductance vs. V_G for low C_{ins} and for high C_{ins}. In the quantum capacitance limit (high C_{ins}), the channel conductance is quantized in units of $4e^2/h$ because occupation of an additional subband adds a $4e^2/h$ channel conductance, as shown in Fig. 6 (a). (The steps are thermally broadened at room temperature.) For low C_{ins}, a much larger gate voltage is required to observe quantization because the Fermi level is pinned at the bottom of the first subband.

Fig. 6(b) shows that in the quantum capacitance limit the transconductance is identical to the channel conductance. The reason is that the nanotube potential is directly modulated by V_G. Increasing V_G by ΔV_G moves the whole E-k down by the same amount, and the energy range which carries current in the +k half increases by $e\Delta V_G$. Similarly, increasing the drain voltage by ΔV_D reduces the energy range that carries current in the –k half by $e\Delta V_D$. In the charge control limit, however, the transconductance is quite different.

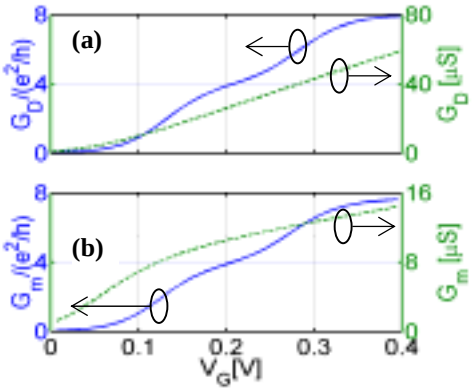

Fig. 6(a) The channel conductance and (b) the transconductance (at V_D=0.4V) *vs.* the gate voltage when C_{ins}=0.4 pF/cm (shown as the dashed line on the right axis) and C_{ins}=90pF/cm (shown as the solid line on the left axis).

COMPARISON TO EXPERIMENT

Top-gated CNTFETs with a nanotube diameter of 2nm and an 8nm thick ZrO_2 gate insulator have been recently reported (3). Figure 7 shows the measured results for a p-channel device along with a fit to a square law FET model from which we deduce a mobility of ≈ 10,000 cm^2/V-s and a series resistance ≈ 60KΩ per contact. Although the mobility is high (a mean-free-path ≈200nm), scattering is important because of the long (~2 μm) channel. The subthreshold swing of 70mV/edcade suggests a low density of ZrO_2/nanotube interface states. The high, positive threshold voltage indicates that the device is a depletion mode FET as in Fig. 1(a). No indication of source exhaustion is observed, so the model of Fig. 1(b) should apply. We cannot rule out the possibility that the device operates as a Schottky barrier FET as in Fig. 1(c), but the geometry is unfavorable for efficient gate modulation of the Schottky barrier.

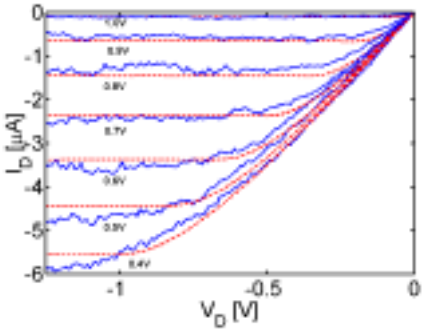

Fig. 7 The experimental I_D vs. V_D characteristics of a planar-gated CNTFET (3). The measured characteristics (solid line) are fit by a square law model with series resistance included (the dashed line).

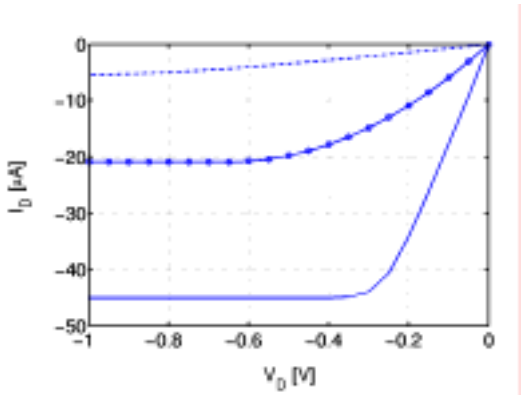

Fig. 8 The theoretical upper limit I_D *vs* V_D of the CNTFET shown in Fig. 7 at V_G*=0.4V*. The solid line assumes ideal contacts with zero series resistance and a ballistic channel. The solid line with symbols assumes zero series resistance but includes the channel scattering. The dash-dot line is the measured characteristics.

Figure 8, which compares the measured performance to the upper limit performance as computed from the model in Fig. 2, indicates that device operates at ~10-15% of its upper limit. Also shown in Fig. 8 is a projection of a square –law intrinsic device with zero series resistance. These results suggest that the on-current can be further improved by: i) by lowering the series resistance, and ii) lowering the channel resistance, which can be readily accomplished by reducing the channel length.

MOSFETs and CNTFETs

To explore the possible role of CNTFETs in future electronic systems, it is important to compare them to Si MOSFETs. Such comparisons are clouded by the need to convert the CNTFET on-current to a per unit width basis. In a planar gate structure, the charge in the nanotube is imaged on a region of the gate that is about 2*d*, where *d* is the nanotube diameter. For the p-CNTFET of Fig. 7, the on-current per unit width expressed this way is ~1500 μA/μm at a gate overdrive of 0.6V. This value is considerably higher than the ~500 μA/μm for a state-of-the-art p-MOSFET at a gate overdrive of 0.6V (19).

The on-current performance advantage of the CNTFET may be due to two reasons: i) the high gate capacitance and ii) improved channel transport. Dividing the nanotube gate capacitance by *2d*, we find an effective gate capacitance of ~5.5 $\mu F/cm^2$ as compared to about ~2.4 $\mu F/cm^2$ for the p-MOSFET (19). The compatibility with high- κ gate dielectrics, therefore, is a definite advantage for CNTFETs. From the measured on-currents, we can also deduce an average carrier velocity at the beginning-of-the-channel. (This comparison removes the ambiguity of the effective width of the CNFET.) We find $\langle v(0)\rangle \approx 7\times10^6\ cm/s$ for the CNTFET and $\langle v(0)\rangle = 3.5\times10^6\ cm/s$ for the p-MOSFET. The improved channel velocity for the CNTFET arises from the increased mobility and the bandstructure of the CNTFET,

The advantage of the larger carrier velocity in CNTFETs remains even if the transistors are near ballistic operation. The thermal velocity of the 2nm-diameter CNTFET is about two times larger than that of a typical Si n-MOSFET. Varying the nanotube diameter changes the band structure and the thermal velocity, but the nanotube has a higher thermal velocity than Si for all physically reasonable nanotube diameters. The advantage for p-type transistors is even larger because the thermal velocity of p-type MOSFETs is only about 1/2 of the n-type MOSFETs, but n and p channel CNTFETs should have the same thermal velocity.

CONCLUSIONS

In summary, we developed a simple model for ballistic transistors, which extends previous models by capturing both the ballistic transport and quantum capacitance limits. CNTFETs present the possibility of achieving both the ballistic and quantum capacitance limits, which the model shows can provide excellent device performance. Presently, CNTFETs still operate well below their upper limit, but with improved contacts and shorter channels, CNTFETs should outperform Si MOSFETs.

ACKNOWLEDEGEMENT

This work was supported by the NSF, grant EEC-0085516, and the MARCO Focused Research Center on Materials, Structures, and Devices which is funded at MIT, in part by MARCO under contract 2001-MIT-887 and DARPA under grant MDA972-01-1-0035.

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